SEVENTH FRAMEWORK PROGRAMME
Information & Communication Technologies

Coordination and Support Action

EU-India Fostering COOPeration in Computing Systems

D3.1: Catalogue of Key Actors

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Executive Summary

This deliverable provides a catalogue of the key actors that are involved in government funded research related to Computing Systems technologies in India and the European Union. The document identifies and analyses research topics having shared interests and potential opportunities for closer collaboration between the EU and India and reports on the organisations that provide funding for Computing Systems related research in India. For each of the Indian organisations that fund research the types of projects that are funded are itemised to provide an overall view of the interests and potential commonalities with research topics in the EU. The report identifies the technology areas receiving both Indian government funding and European Commission funding, along with technology funding areas that are specific to each region.

The focus is towards providing insight into the Indian organisations involved in funding and carrying out Computing Systems research as there is already substantial information publicly available from the European Commission concerning Computing Systems research programmes and funded projects in the EU. A set of considerations are also noted in anticipation of possible joint research and development actions between the EU and India.

Table of Contents

1 Introduction

1.1 Purpose of this deliverable

This deliverable has been developed by the EUINCOOP Project to catalogue the key actors involved in government funded research in India and the European Union (EU), and to identify research topics having shared interests and potential opportunities for closer collaboration. The deliverable reports on the organisations that provide funding for Computing Systems related research in India, describes the types of projects that are funded, and identifies common technology areas receiving both Indian government funding and European Commission (EC) funding, along with technology funding areas that are specific to each region.

The deliverable has a focus towards providing insight into the Indian organisations involved in funding and carrying out Computing Systems research, which complements the rather substantial information already publicly available from the EC concerning EU Computing Systems research programmes and funded projects. The deliverable is targeted for use by different constituencies and their expected use and related sections of this deliverable are described in Section 2.

The identification of key actors is one of the early steps in the EU-INCOOP work programme. These organisations are expected to be the most involved in further work within the project of identifying areas of common research, encouraging closer collaboration amongst EU and India funded projects, and creating an opportunity for more coordinated funding of Computing Systems research between India and the EU in technology areas that have strategic importance to both regions.

1.2 Structure of this document

This deliverable is structured as follows:

- Section 2 provides guidance on how the document can be used by different EU and Indian constituencies
- Section 3 describes the Indian organisations that provide research funding for Computing Systems technologies and the procedures they follow
- Section 4 lists the various research projects funded in India related to Computing Systems technologies
- Section 5 describes the Indian organisations involved in carrying out India government funded research in Computing Systems technologies
- Section 6 analyses EU funded projects to identify those related to projects funded in India and also identifies key actors involved in EU funded projects
- Section 7 provides an analysis of the research technology competencies in Computing Systems for both India and the EU
- Section 8 concludes with further aspects to be considered when establishing coordination of funding for projects between India and the EU

In several sections website links are provided within this document where additional information is available.

1.3 Scope

This deliverable has been developed to achieve specific objectives within the EU-INCOOP project under the FP7 ICT Programme, and in particular related to the Computing Systems objective within the European Commission's ICT Work Programme. The time horizon for the information provided is aligned with FP7 (2007-2013). In particular, the actors identified are currently involved in funding or carrying out Computing Systems research; and the research projects listed have been carried out during the FP7 timeframe or are currently ongoing.

The EU-INCOOP partners note that there are limitations in describing India government funded projects when compared to those funded in the EU. The funding in India is spread across multiple government ministries, and there is no equivalent to the EC's CORDIS system in India that provides a centralised source for information concerning India government funded projects. The Indian project information provided has been collected from a combination of public sources and personal contacts of the EU-INCOOP partners. Details of some project attributes (e.g. project funding levels) were in some cases unavailable, or considered too unreliable to include in this document.

In carrying out the analysis of projects both in India and the EU, the partners have focused on Computing Systems related research and development projects. While support actions and other coordination projects play an important role in both India and the EU, this deliverable focuses on the technology research and development work in both regions. EU funded STREPs and IPs and their Indian equivalents were included in the investigations and analyses, while EU funded CSA's and their Indian equivalents were generally not considered.

Regionally funded projects in India and nationally funded projects in Europe have not been considered for the analysis. This is to ensure comparative consistency within the analyses as well as in recognition that a joint funding initiative between the EU and India would be established between central government institutions rather than at the regional or national level.

In particular, embedded systems projects under the ARTEMIS Joint Undertaking in the EU have been included in the analyses primarily for the identification of key actors in Europe. The reason for this focus is:

- the research agenda and priority of project funding is set by an industry association and the programme is partially funded by the participating actors
- the majority of funding for ARTEMIS projects comes directly from EU member states
- several EU member states do not participate in ARTEMIS or the funding provided is at such low levels that it limits participation of actors from those regions
- many member states limit either research or industrial actor participation in ARTEMIS projects, which skews the types of organisations that participate in ARTEMIS projects

The project has focused its analyses on EU Computing Systems projects directly funded by the European Commission as this is analogous to the Computing Systems projects in India that are funded by the Indian government. There are projects funded at the state level within India that would in some ways be analogous to those funded by the ARTEMIS Joint Undertaking and other national projects in the EU. However, an analysis of state level projects in India and the EU is not within the scope of the EU-INCOOP project as a joint funding initiative between the EU and India would most likely be established between central government institutions rather than at the regional or national level.

1.4 Contributors

The deliverable was prepared with contributions from all of the EU-INCOOP partners, each playing an important role in preparing the contents:

- IISc investigated the Indian organisations providing funding including their governance and project funding procedures
- CDAC investigated the projects related to Computing Systems that have been funded by the Indian government
- ITSMA investigated the Indian partners involved in Indian funded projects as well as non-government funded projects addressing Computing Systems research
- KYOS identified the EU Computing Systems projects and analysed the partners involved in EU funded projects
- FORTH and TOG carried out the technical analysis of all the EU and Indian funded research projects to identify commonalities and areas for possible collaboration
- TOG provided the overall structure, coordination and editing of this deliverable, while FORTH carried out reviews and quality control

The development of this document required the close collaboration amongst the project partners, especially due to the often limited availability of detailed information concerning projects funded by the Indian government.

2 Using this catalogue

This deliverable is intended to catalogue information that is beneficial for several different constituencies in both the EU and India. In developing this document the following target audiences were identified and the contents have been structured accordingly:

- Indian research organisations
- Indian Government organisations
- European research organisations
- European Commission

Guidance on the intended use of this document for each target audience and the relevant sections is provided in Table 1.

Audience	Intended Use	Relevant Section(s)
Indian research organisations	Providing information about EU funded projects that are related to Indian projects	Section 6
	Understanding the size of projects and participation of actors in EU funded research projects	Sections 6 and 7
	Identification of key actors involved in EU funded research projects for future collaboration	Section 7
Indian Government organisations	Identification of EU funded projects where collaboration with Indian projects could be encouraged	Section 6
	Identification of research topics that are common between India and the EU	Section 8
	Identification of key EU actors to potentially include in discussions or consultations concerning India's strategic research agenda	Section 7
European research organisations	Identification of India funded projects related to EU funded Computing Systems projects	Section 4
	Identification of potential sites and partners in India for evaluating EU funded research technologies	Section 4
	Identification of leading research organisations in India to invite to participate in new proposals for EU funding	Section 5
European Commission	Information about the topics addressed by India funded projects	Sections 3 and 4
	Information about Indian government organisations that fund Computing Systems related research	Section 3
	Information about Indian organisations involved in India funded research projects	Section 5
	Identification of research topics that are common between India and the EU	Section 8
	Identification of key Indian actors to potentially include in discussions or consultations concerning the EC's strategic research agenda	Section 5

Table 1: Guide to using the catalogue for target audiences

The document also includes website links within the relevant sections where additional information is available for each of the target audiences.

3 Funding sources for ICT research in India

3.1 Overview of Indian research funding

A key attribute of India government funding of Computing Systems research and development is that the funding is decentralised. Several government organisations provide financial support according to the needs of driven from three main areas:

- Science and Technology
- Medicine
- Social Sciences

Each area has an associated government ministry and each of the funding organisations that provide financial support report directly to the respective ministry.

Funding in India for research projects is granted following a two way procedure:

- Bottom up approach: The researchers and scientists of government funded research organisations apply for grants by presenting their project ideas to a committee of appointed experts belonging to the field in which the proposals are made.
- Top down approach: The funding agencies act on predetermined national priorities in certain areas usually suggested by a Programme Advisory Committee (PAC) or Science and Education Research Council, which are bodies comprised of researchers, scientists, and policy makers from ministries. These groupings publish a call for proposals in the chosen areas. The information is published on the websites and an information circular is usually circulated to all the major heads of the Indian scientific institutions to respond to the calls.

The system for funding of science and technologies in India is shown in Figure 1. The system involves a combination government and industry funding where many government funded organisations also received substantial funding from the private sector, not only from within India, but also private industry from abroad.

Figure 1: Structure of Science and Technology funding in India

Within the Indian Government itself there are several ministries and departments involved in funding research and development projects as shown in Figure 2.

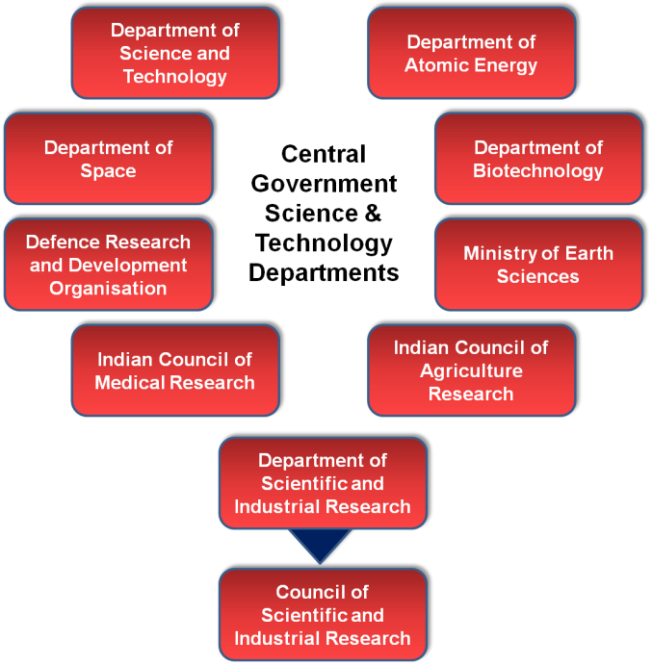

Figure 2: Indian Government Science and Technology Departments

The government of India funds research and academic institutes through various departments such as the:

- Department of Science and Technology
- Department of Biotechnology
- Indian council for Medical Research

- Indian council for Agricultural Research
- Department of Space
- Department of Atomic Energy
- Defence Research and Development Organization
- Department of Scientific and Industrial Research
- Department of Information Technology

Four of these major departments are involved in the promotion of research and technology in both fundamental and applied research of Engineering and Life Sciences broadly, and Computing Systems in particular for the country:

- Department of Science and Technology
- Department of Biotechnology
- Department of Information Technology
- Ministry of Earth Sciences

In addition to these organisations, the Centre for Scientific and Industrial Research (CSIR) with 39 laboratories doing research and technology development in various fields of science and technology (the largest R&D organisation in India), is also involved in supporting fundamental and applied research. A description of each of these organisations is provided below.

3.2 Department of Science and Technology (DST)

The Department of Science & Technology plays a pivotal role in promotion of Science & Technology in the country. The Department has wide ranging activities ranging from promoting high end basic research and development of cutting edge technologies on the one hand, to service the technological requirements of the common man through development of appropriate skills and technologies on the other. DST was establishes with an objective of promoting new areas of science and technology and to play the role of a nodal department for organising, coordinating and promoting science and technology activities in the country.

A key initiative for the DST is in the area of Supercomputing. The government, realizing the need to keep pace with the emerging and the developed world and regain its lost edge in supercomputing has earmarked €750 million to establish a fabrication facility to create next generation computers.

The programme coordinator Prof Balakrishnan of IISc said "There is an urgency among scientists and policy-makers that India has fallen behind in supercomputing. In Supercomputing, India is currently ranked 140th in the world; it was ranked third in 2007. The fall is drastic and alarming and has to be arrested immediately. IISc and DST will work to revive the country's original strength." Professor Balakrishnan, is a member of the Prime

minister's scientific advisory committee and is one of the key members coordinating the project in supercomputing.

"Supercomputing involves capacity building, and not just fabrication and setting up of computers. The capacity building requires right technology - range of sensors, plenty of intelligence related equipment, and hardware. Industries will employ specialised technology researchers to build technology and equipment. Overall, the project should be a vehicle for growth of the technology industry," Balakrishnan explained.

This Project offers tremendous scope for scientists, researchers within India and collaborative opportunities internationally.

While Indian supercomputer PARAM 10,000 is already successfully functioning at the Russian Indian Centre for Advanced Computing in Moscow; Indian Supercomputer PARAM PADMA RU is being jointly developed in Russia. Projects addressing development of software for applications like Computational Fluid Dynamics, Seismic Data Processing and Development of Parallel Compiler are also implemented.

DST on the advice of SERC supported projects on development of earthquake risk analysis system for RCC frame structure on Grid computing project in 2010 which is one of the priority areas proposed by SERC. Sri Govindram Seksaria Institute of Technology and Science (SGSITS) – Indore and C-DAC, Pune executed the project focusing on building models for the analysis of the data while C-DAC expertise in high performance computation will facilitate in utilizing these models by developing algorithms for the same. These projects and initiatives show the government's commitment towards supercomputing and high performance computing in general. Projects related to Bioinformatics also have a priority when it comes to funding.

3.2.1 Governance

DST comes under the Ministry of Science and Technology which is headed by Shri Vilas Rao Deshmukh. The Minister of State for Ministry of Science and Technology is Dr Ashwini Kumar who directly reports to the minister. Dr T Ramasami is the Secretary and heads all scientific groups, administrative functions, scientific services, autonomous institutions.

The Science and Engineering Research Council (SERC) was established in 1974 and is an apex body through which the DST promotes research and development programmes in newly emerging and challenging areas of science and engineering. SERC is composed of eminent scientists, technologists drawn from various universities/national laboratories and Industry. This Council is assisted by Programme Advisory Committees (PACs) in various disciplines of Science & Engineering.

SERC had earlier identified specific areas of research known as the Thrust Areas through the mechanism of organising a series of national workshops in several disciplines. More recently, the PACs of the SERC have deliberated on updating these Thrust Areas and identifying new challenging areas for support in the 21st century.

A few examples of the broad areas identified by the SERC are:

- Molecular Biophysics
- Habitat fragmentation biology

- Chronobiology
- Plant animal relationships
- Small permanent magnet machines
- Smart sensors, optical communication
- Use of hydrogen as fuel, watershed management
- High precision manufacturing
- Design of VLSI circuits
- Sensors integrated robotics system
- Synthesis and structure
- Organometallic and cluster chemistry
- Quantum optics and basic laser physics
- Non-linear optics
- Physics of biological systems
- Evolution of India crust
- Study of earthquake processes
- Climate observation and modelling
- Severe weather system

The study of earth quake processes, climate observation, and modelling severe weather systems fall under the Computing Systems domain, which is one of the Thrust Areas of the SERC.

3.2.2 Level of funding

Although separate amounts of funding for a specific Thrust Area are not provided, the overall budget for research and development projects in 2010 was €240 million in science and technology related areas. The government plans to double its research and development funding for the 12th plan (similar to the EC's Framework Programme) in 2012-2017. The corridors of the government do spell out clearly that funding for a high impact project with wide spread benefits to a large section of the society will not have any constraints with the right actors implementing a well laid out plan.

3.2.3 Funding mechanism and procedures

Once a call is published and circulated, proposals are invited from experienced research/academic institutes who have the necessary expertise to execute the project. The time between the published call and deadline is usually 3 months. The proposals are vetted with the PAC in the chosen area. Out of the submitted proposals, depending on the relevance and impact of the projects, a few proposals will be invited for negotiation of the budget. Usually the whole process takes about 3-4 months time. Once the proposal is

approved and accepted, the sanctioning of funds will take nearly 3-4 months further, which is when the proposal attains the project status.

Shorter, one year project proposals are accepted in certain areas of research (e.g. engineering sciences and life sciences) and the proposals are evaluated in a similar manner following the internal procedures of vetting with expert committees and grading them on a 10 point scale of different parameters.

This same procedure is followed also by Department of Biotechnology (DBT) and the Department of Information Technology (DIT) and their respective PACs, with only minor variations in evaluation procedures

3.3 Department of Biotechnology (DBT)

In the over ten years of its existence, the department has promoted and accelerated the pace of development of biotechnology in India. Through several research and development projects, demonstrations and creation of infrastructural facilities, a clear visible impact in this field has been seen. The department has made significant achievements in the growth and application of biotechnology in the broad areas of agriculture, health care, animal sciences, environment, and industry.

A unique feature of the department has been the deep involvement of India's scientific community through a number of technical task forces, advisory committees and individual experts in identification, formulation, implementation and monitoring of various programmes and activities. DBT has dedicated efforts towards establishing the Biotechnology Information System (BTIS) and the National Bioinformatics Network

It has been proposed to expand the High Speed BIOGRD INDIA (VPN) for the BTISnet for fast and reliable connectivity to achieve nearly instantaneous access to the biological databases by the scientific community. Pooling of hardware infrastructure on this platform would also reduce the expenditure on high-end computers at different places, which is one of the important motivations behind the project. Access to on-line journals will be introduced as part of this network. Growth of biotechnology has accelerated particularly during the last decade due to path breaking advancements in biology and new technologies that produce large high quality data. One such advancement is the high throughput full genome sequencing projects, including human genome, which have produced very large data. The analysis of such large data and extraction of knowledge from this data is possible only with the help of new algorithms and computational intensive techniques using high performance computing.

The principal aim of the bioinformatics programme is to ensure that India emerges as a key international player in the field of bioinformatics; enabling a greater access to wealth of information created during the post-genomic era and catalyses the country's attainment of lead position in medical, agricultural, animal and environmental biotechnology. The motivations for the Indian government to undertake this initiative is to:

- undertake advanced research in frontier areas of bioinformatics and computational biology

- develop world class human resource in bioinformatics
- establish effective academia-industry interface
- pursue and promote international cooperation with leading institutions, organizations and countries in the world.
- create world-class platforms for technology development, transfer and commercialization

The Supercomputing Facility for Bioinformatics & Computational Biology (SCFBio) at IIT Delhi was created in July 2002, with funding from the Department of Biotechnology, Department of Science & Technology, and Council of Scientific & Industrial Research. The objectives of the facility are to:

- establish a nodal facility for supercomputing, accessible to the Bioinformatics community
- develop novel scientific methods and new software for genome analysis, ab initio protein structure prediction and active site directed drug design

The facility is working on all major aspects of Bioinformatics viz. Genome Analysis, Protein Structure Prediction and Drug design.

3.3.1 Governance

Both DBT like DST (see Section 3.2 above) comes under the Ministry of Science and Technology which is headed by Shri Vilas Rao Deshmukh. The Minister of State for Ministry of Science and Technology is Dr Ashwini Kumar who directly reports to the minister. Dr T Ramasami is the Secretary and heads all scientific groups, administrative functions, scientific services, autonomous institutions.

Department of Biotechnology is organized on modern lines of management, reducing vertical hierarchy and promoting horizontal interaction amongst the scientific groups and officers. The Department is being advised by two apex level committees: Scientific Advisory Committee (SAC-DBT) and Standing Advisory Committee – Overseas (SAC-O). These committees review the ongoing programmes and suggest new and emerging areas that could be supported.

The DBT has set up task forces and expert committees with the involvement of eminent and active scientists from all over the country to advise on the identification of thrust areas in Biotechnology for financial support. As a result biotechnology has received a significant upswing of support from the Government of India.

There are fifteen task forces and various expert/steering committees of the department who meet two or four times during the year to review and monitor the ongoing projects and also consider new proposals in the priority areas. A special thrust has been given during the year on formulation and funding of new projects – especially multi-institutional and interdisciplinary project, as per the priority of the 10th Plan (similar to the EC's Framework Programme).

3.3.2 Level of funding

DBT has an annual budget of €150 million with projects funded according to the proposals they obtain from the researchers and scientific community. Adequate budgets according to the needs of the project are provided. There is no allocation of budget by topic and any project which is from a high priority area will be funded as per the project requirement. This approach does run the risk of research fragmentation, but if a project with several eligible partners come together to implement a proposal it will be funded by the agency.

3.4 Department of Information Technology (DIT)

The Department of Information Technology since its inception has been giving importance to research and development. Promotion of research & development efforts in electronics and related fields in the country has been one of the major activities of Department of Information Technology.

3.4.1 Governance

Unlike the DST (see Section 3.2) and the DBT (see section 3.3), the DIT comes under the Ministry of Communication and Information technology which is headed by the Minister and Minister of State. The reporting structure within the DIT is shown in Figure 3.

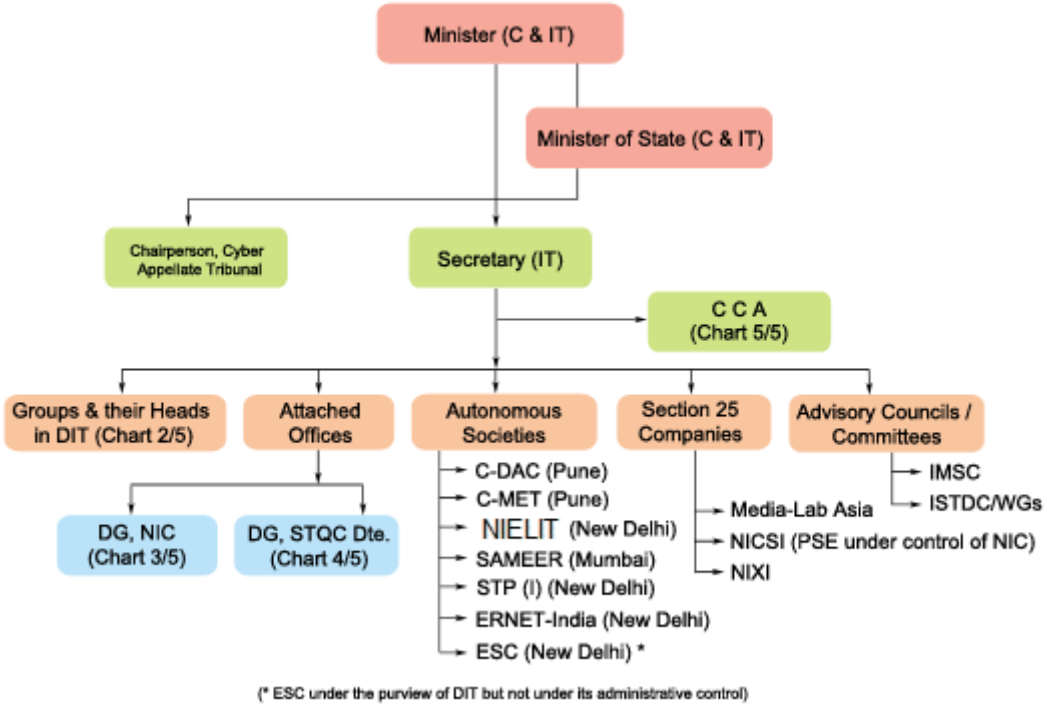

Figure 3: Structure of the Department of Information Technology

The Secretary heads the various groups, societies, and councils. DIT identifies the research thrust areas on the advice of the Advisory councils/committees and working groups.

3.5 Ministry of Earth Sciences (MOES)

The mandate of the Ministry of Earth Sciences is to provide the nation with best possible services in forecasting the monsoons and other weather/climate parameters, ocean state, earthquakes, tsunamis and other phenomena related to earth systems through well-integrated programmes. The ministry supports science and technology related to exploration and exploitation of resources. The objective of this ministry is to play a nodal role and equip the nation to save life, property, to prepare the nation for natural disasters using science and technology, and improve its infrastructure by funding the requisite research areas.

MoES aims to create a framework for understanding the complex interactions among key elements of the Earth System, namely ocean, atmosphere and solid earth, by encompassing national programmes in Ocean science, meteorology, climate, environment and seismology.

The various Units under the Ministry of Earth Sciences are:

- India Meteorological Department (IMD)
- National Centre for Medium Range Weather Forecasting (NCMRWF)
- Indian Institute of Tropical Meteorology (IITM) Pune, and Earthquake Risk Evaluation Centre (EREC) under the Atmospheric Sciences and Seismology sector
- National Institute of Ocean Technology (NIOT) Chennai
- National Centre for Antarctic & Ocean Research (NCAOR) Goa
- Indian National Centre for Ocean Information Services (INCOIS) Hyderabad
- Integrated Coastal and Marine Area Management Project Directorate (ICMAM-PD) Chennai
- Centre for Marine Living Resources & Ecology (CMLRE) Kochi under the Ocean Science & Technology sector

Those units that are carrying out research in Computing Systems related areas are further described below.

NCMRWF developed numerical weather forecast models of high resolution have proved to be viable tools for the production of weather forecast in the medium range (3-10 days in advance). Since inception, National Centre for Medium Range Weather Forecasting (NCMRWF) has been working on development of such models and data assimilation techniques to provide meteorological forecasts for agro-advisory purposes and other applications. Supercomputing and high performance computing are the focus areas of this centre.

The India Meteorological Department (IMD), established in 1876, is the national meteorological agency of the country. It is responsible for monitoring forecasting weather conditions in different scales of time. It has a network of observatories covering the landmass of the country and its surrounding sea areas from where ground-based, airborne and satellite observations are routinely taken. The services of IMD are utilized in almost all

walks of national life and also provided to the international community under the charter of World Meteorological Organization.

The computational power requirements by this department are huge and the quantum of presence of this requirement is inadequate. This gap has to be filled to give early warning signals of natural disasters, so the department encourages and supports projects related to high performance computing that would impact this need.

The Indian Institute of Tropical Meteorology (IITM) was separated from the India Meteorological Department in 1962 and established as a Centre for Research. It now functions as the National Centre for basic and applied research in Tropical meteorology and Atmospheric Sciences, in all its aspects, with special reference to the tropics and sub-tropics.

Indian National Centre for Ocean Information Services (INCOIS) was set up with its head quarters at Hyderabad in February 1999. The Centre is responsible for dissemination of Ocean related information to a variety of users. It is also the nodal agency for running the Tsunami and Storm Surge Early Warning System started in October 2007. The information it provides on ocean waves, swell, etc. are found quite valuable to Navy, Coast Guards, and Merchant Ship. Similarly, Fishing Zone Advisories are utilised by large number of fishermen.

Of particular interest to INCOIS are high performance computing and related research areas of computing systems for Weather Prediction / Early Cyclone Warning, Ocean State Model Calibration, Climate Research, Satellite Data Validation, and Port Development / Navigational Use.

3.5.1 Governance

The Ministry of Earth Sciences, like the DST (see Section 3.2) and the DBT (see section 3.3) comes under the purview of Minister for Science and Technology, Mr Vilasrao Deshmukh, and Minister for State, Dr Ashwini Kumar. Dr T Ramasami is the Secretary and heads all scientific groups, administrative functions, scientific services, autonomous institutions. The organisational structure of the MOES is shown in Figure 4.

Shri Vilasrao Deshmukh
Minister
Ministry of Earth Sciences and Minister for Science and technology

Secretary
Ministry of Earth Sciences
&
Chairman of Earth Commission

DIRECTOR

Admin Scientists/ Technology Groups

Project Scientists

Figure 4: Structure of Ministry of Earth Sciences

The MOES functions through its units/centres in realizing its mission. The centres are funded by the MOES. Each centre is headed by the Director, the technology groups, and the administrative functions are followed in the hierarchy.

3.6 Centre for Scientific and Industrial Research (CSIR) Labs

CSIR or the Centre for Scientific and Industrial Research is the largest autonomous R&D organisation in India with 39 laboratories doing research and technology development in various fields of science and technology. Centre for Electronics Engineering Research Institute (CEERI) is one of the 39 labs of CSIR. CEERI was established with a mandate to:

- carry out R&D in electronic devices and systems
- assist industry in technology absorption, upgradation and diversification
- provide R&D services to industry and users in design, fabrication and testing
- provide technical services for specific needs towards product development, precision and quality in semiconductor devices and electronic systems

CEERI is involved in several projects relating to computing systems under its electronics systems area.

CEERI is headed by the Director, under whom the research groups, research council and the admin functions operate. The R&D Planning and the business development come directly under the Director, while the research group heads operate with a fair degree of autonomy when it comes to R&D projects and planning.

The Council for Mathematics Modelling and Computer Simulation (CMMACS) was established by CSIR in 1988. The thrust areas of R&D of the centre are modelling of hazard environments, pollution, climate change, as well as modelling for new drugs.

An important program initiated by the centre in the wake of the destructive earthquake was the modelling of the crustal strain in the Indian crust using GPS receivers. The work carried out yielded repeatable and accurate results which are now being replicated to measure the velocity of the Indian plate with respect to that of the Eurasian plate as well as the rotation of the earth's axis. All of this was made possible through in-house computational capabilities.

3.6.1 Governance

CMMACS policies and programmes of the centre are approved and monitored by a high level advisory committee under the chairmanship of the Director General of CSIR, comprising members from various academic, industrial and research institutions.

4 Government funded research projects in India

The five main sources for Indian Government funding of ICT research projects support a wide range of initiatives and topics. Some of these are nationally focused addressing such topics as improving India's Grid computing infrastructure, while others are addressing the advancement of strategic technologies to benefit India's global market position such as technologies for Bioinformatics, while many are new technologies developed to address the needs within specific application domains.

Table 2 provides a listing of the Indian projects that are related to Computing Systems that have been operational within the FP7 timeframe, or are ongoing. The projects are grouped by funding source to provide an overall impression of the types of projects related to Computing Systems each Indian Government organisation supports. The Indian funding sources are the following:

- DIT – Department of Information Technology
- DBT – Department of Biotechnology
- MoES – Ministry of Earth Sciences
- DST – Department of Science and Technology
- CSIR – Centre for Scientific and Industrial Research Labs

Each of these organisations are described in detail in Section 3 and an analysis of the listed Indian project topics in comparison to EU funded projects is provided in Section 8.

Funding Source	Area	Project Name	Objective	Organisation	Status	Funding (Euros)	Duration
DIT	Bio-Informatics	Bio-informatics Resource and Application facility (BRAF) Phase I	Setup a Grid-enabled Bioinformatics Resource (Computing Power, Databases and the Software)	C-DAC Pune	Databases and software including teraflop computing power, terabyte storage with 10 Mbps bandwidth along with Bioinformatics Applications like Smith Waterman, BLAST, CLUSTAL W, Amber et al is provided.		
DIT	Bio-Informatics	Development of Computational Workflow for High Throughput Genome Analysis	Establish a state-of-the-art High Throughput Genome Analysis facility using a computational workflow environment	C-DAC Pune	Under Trial		
DIT	Bio-Informatics	Internet Computing Software to Detect Various Repeats in Genome and Protein Sequences	Creating high-end internet computing engines to analyze comprehensive biological data available as open literature. Developing powerful computing engines will be one of the major goals.	IISc Bangalore	An algorithm for sequentially separated motifs in Biological sequences has been developed, research paper published in the current Science issue and efforts are on to develop web server for the same.		
DIT	Ubiquitous Computing	Establishment of National Ubiquitous Computing Research	Create a R&D base in the multi-disciplinary areas of Ubiquitous Computing	C-DAC Bangalore		298K	2007-11

Funding Source	Area	Project Name	Objective	Organisation	Status	Funding (Euros)	Duration
		Centre	(UbiComp)				
DIT	Ubiquitous Computing	Establishment of National Ubiquitous Computing Research Centre	Advanced Ubiquitous Computing Research (UbiComp) - focus is on specific domains of UbiComp such as sensing and actuation, context awareness, real-life applications, security & trust, mobile computing and embedded systems. The project aims to integrate the research work in Wireless Sensor Networks (WSN) into an Adaptive Framework that would facilitate faster development of WSN applications. Another major objective of the project is to provide a framework for hosting solutions to various security and trust issues in an UbiComp environment. The UbiComp project also aims at significant efforts in research of blending the UbiComp and Grid Computing (GrUb Computing) domains to facilitate anytime, anywhere learning that would	C-DAC Centres (Hyderabad, Chennai, Bangalore, Trivendrum, Mohali, Kolkatta)		2.98M	2012-15

Funding Source	Area	Project Name	Objective	Organisation	Status	Funding (Euros)	Duration
			integrate e-Learning and m-Learning thus leading to u-Learning environment.				
DIT	Ubiquitous Computing	Design and Development of Ubiquitous Computing Test Bed and UC Applications	Develop efficient test-bed architecture for ubiquitous applications and a framework for testing UC applications having standard configurations	IISc Bangalore	Currently many of the systems have already been developed.		
DIT	Scientific Computing	Coupled Climate Models on Grids at SERC, IISc Bangalore	Build techniques for The efficient executions of different model components of a coupled climate model on different sets of resources in a Grid Environment and compare the various advantages of Grid executions with the execution of all the model components in the resources available in one site	SERC, IISc Bangalore	Currently Coupled Climate System Model (CCSM) consisting of four inter-connected subcomponents, namely the atmosphere model, the ocean model, land surface processes model and a model for sea-ice have been ported on a single parallel system and testing is under progress in grid environment with atmosphere, ocean, land surface processes and sea-ice models on separate clusters.		
DIT	Scientific Computing	National grid computing initiative –	The scope of work includes research in Grid	C-DAC and collaborators:	Currently GARUDA has 65+ partners , 30+	7.3M	2009-12

Funding Source	Area	Project Name	Objective	Organisation	Status	Funding (Euros)	Duration
		GARUDA Research Activities.	environment such as Grid Virtualization, build a national grid test bed for scientific community & applications, Portal for single point access to grid resource, Semantic/ knowledge Grid, Grid Scheduling, data-grid solution, Grid resource monitoring, Trusted Grid Computing along with addressing the requirement for producing high quality trained R&D manpower.	SAC Ahmedabad , IIT Mumbai, OSDD, IISc Bangalore	location connected with 1 GBPS backbone link. GRID tools developed: monitoring tool, Grid Debugger, Distribution Package, Automated Grid service. Several successful applications from different disciplines are operational.		
DIT	Scientific Computing	Scientific Cloud for HPC	Scientific Cloud for HPC Applications including System Software & Middleware Architecture for Scientific Cloud, Large Data Transactions Handling capability on Cloud, Virtualizations, Licensing Issues, etc. Research for storage solution, middleware, scientific application for SaaS on scientific Cloud. Private cloud environment is established with open source tools in C-DAC and	C-DAC Centres (Bangalore, Chennai, Pune, Hyderabad, Mhali)	Research for storage solution, middleware, scientific application for SaaS on scientific Cloud is in progress	3.28M	2011-13

Funding Source	Area	Project Name	Objective	Organisation	Status	Funding (Euros)	Duration
			value added components will be developed, customized and integrated in to the cloud.				
DIT	Scientific Computing	Implementation of Bio-Inspired Distributed Artificial Neural Network (DANN)	Use of distributed computing and Grid resources to implement a bio-inspired model of the neural network and its application.	Guwahati University	Project is underway		
DIT	Scientific Computing	Development of Analytical Tools for Large Scientific Knowledge Bases	To create Web Based Vedic and Sanskrit Knowledgebase, develop Analytical and Search Capabilities and deployment in Garuda Grid environment	C-DAC Bangalore	Completed	75K	2008-10
DIT	Free Open source Software	National resource Centre for Free/Open Source Software (NRCFOSS Phase II)	Development of SaaS stack delivery model based on FOSS Service Oriented architecture and its implementation for the Linux kernel, middleware , Integration and Development of Common Desktop development infrastructure , Setting up of Centre of Excellence for Mobile Internet devices based on BOSS Linux , Development and enhancement of NRCFOSS	C-DAC Centres (Chennai, Mumbai, Hyderabad, Delhi), Anna University, IIT Mumbai, IIT Chennai	Development of SaaS model based on FOSS	3.28M	2009-12

Funding Source	Area	Project Name	Objective	Organisation	Status	Funding (Euros)	Duration
			portal which will become a platform where multidisciplinary organizations involved in FOSS collaborate , Enhancing accessibility for FOSS Desktops , Setting up of GCC Resource Centre , HRD in FOSS – Phase II promotion , Open Source Walk-in e-Learning solutions Laboratory with focus on standards compliance and Offering Certification course in FOSS , Development of FOSS Knowledge Bank/Repository for scientific/education/e-Governance applications , Further additions and enhancements to BOSS/Linux specific to education & scientific domain				
DIT	Medical Electronics & Telemedicine	Healthcare Information Store	Technology Development for building distributed, scalable, and reliable Healthcare Information Store	C-DAC Pune			
DIT	Medical Electronics &	Medical Image Analyser for Cervical	Development of Medical Image Analyser for Cervical	C-DAC Thiruvanantha			

Funding Source	Area	Project Name	Objective	Organisation	Status	Funding (Euros)	Duration
	Telemedicine	Cancer	Cancer (Cervi SCAN)	puram, IIT Kharagpur, RCC Thiruvanantha puram			
DIT	Medical Electronics & Telemedicine	Data Management System for Oncology	Development of Data Management System for Oncology	C-DAC Thiruvanantha puram			
DIT	Medical Electronics & Telemedicine	Telemedicine Applications	Developing of a Web Enabled Medical Information Access Using Handheld Devices in a Wireless Environment for Telemedicine Applications	IIT Kharagpur, WECS Kolkata			
DIT	Medical Electronics & Telemedicine	Mobile Tele-oncology System	Development and Implementation of ICT based Mobile Tele-oncology System for extending the coverage of ONCONET, Kerala	C-DAC Thiruvanantha puram			
DIT	Innovation Promotion Projects	Developing Plagiarism Detection Engine for Detecting Source Code Plagiarism at Amrita Vishwa Vidyapeetham	Extend DVIAT (Plagiarism detection engine developed at Amrita University) to detect source-code plagiarism.	Amrita Vishwa Vidyapeetham	The project has been recently initiated and the project team is in process of setting up infrastructure and manpower.		
DIT	Supercomputing	Russian - Indian center for Advanced computing Research (RICCR)	The ongoing collaboration resulted in the Governments of Russia and India deciding to set up a Russian Indian Centre for Advanced Computing Research (RICCR)	C-DAC Pune	Further details can be found at www.riccr.com		

Funding Source	Area	Project Name	Objective	Organisation	Status	Funding (Euros)	Duration
			in Moscow nodalised by the Indian Dept. of Science and Technology and Russian Academy of Sciences				
DIT	Supercomputing	National Param supercomputing Facility	100 GF Supercomputing facility to support scientific application	C-DAC Pune		4.47M	2006-08
DIT	Supercomputing	C-DAC's Terascale supercomputing Facility	4 TF supercomputing facility to support scientific application	C-DAC Bangalore		447K	2006-07
DIT	Supercomputing	C-DAC's Terascale supercomputing Facility	20 TF supercomputing facility to support scientific application	C-DAC Bangalore		149K	2012-14
DIT	High Performance Computing	HPC software	Supports the development and execution of sequential, message passing and data parallel programs and allows the ensemble of workstations to be viewed as independent workstations, cluster of workstations, or as a massively parallel processor system.	C-DAC Bangalore	PARMON - Cluster monitoring tool., KSHIPRA - Scalable Communication Substrate for Cluster of Multi Processors, C-PFS - Scalable Parallel IO for UNIX Clusters, DIViA (Debugger with Integrated Visualizer and Analyzer), F90IDE - A Comprehensive Development Environment for Fortran, C-MPI - Optimized MPI for Cluster of Multi Processors, RMS -		

Funding Source	Area	Project Name	Objective	Organisation	Status	Funding (Euros)	Duration
					Optimal Resource Management for Clusters.		
DIT	Ubiquitous Computing	C-DAC wireless sensor node	Monitor environmental conditions and to bridge the gap between the physical and the digital world.	C-DAC Bangalore	Used by applications as Industrial and home automation, Large scale sensor networks, Acoustic, vibration and other high speed sensor data	307K	2007-10
DIT	Real Time System Software	EREB – Phase II Eastern Region Electricity Board, Kolkata	Design and implement of Fault Tolerant System and Energy Management System at RLDC	C-DAC Bangalore	Developed and implemented		
DIT	Real Time System Software	Steel Authority of India Ltd., Ranchi	Design and implementation of a Central System (RTU) for a Plate Mill.	C-DAC Bangalore	Developed and successfully implemented		
DIT	Real Time System Software	National Thermal Power Corporation Limited, Lucknow	To provide Online Data / Text Transfer of NRLDC Data to NTPC	C-DAC Bangalore	Developed and successfully implemented		
DIT	Ubiquitous Computing	Smart PARKing	Aim to develop automation of vehicle parking, guiding the drivers for parking, support advance parking and report generation to facilitate admin of the parking system	C-DAC Hyderabad	Successfully implemented	968K	2007-11
DIT	Ubiquitous Computing	u-Agri	Aim to automate weather data acquisition from fields thereby facilitating Decision Support Advisories	C-DAC Hyderabad		968K	2007-11

Funding Source	Area	Project Name	Objective	Organisation	Status	Funding (Euros)	Duration
DIT	Supercomputing	EU-India Grid	Aims at interconnecting the Grid infrastructure in Europe (EGEE) and India for the benefit of Science applications	ERNET and the members of the consortium are "Institute Nazionale di Fisica Nuclear, ITALY", "Metaware, PA, ITALY", "GARR, ITALY", "International Centre for Theoretical Physics", "Cambridge University, UK", "SAHA Institute Calcutta, India"		60K	2008-11
DBT	Bio-Informatics	Bioinformatics & Sun Co-E	Data Centre provides bioinformatics services in the form of browsing biomolecular sequence databanks, macromolecular structure databanks, genome and other useful databases. It provides services for the comparison and analysis of sequence/structure/genome	Centre for DNA Fingerprinting and Diagnostics (CDFD) Hyderabad, Sun Microsystems Inc., USA	Service is used for activities such as: Genome analysis, Functional Genomics & Systems Biology; Data mining and analysis of DNA Micro array, Proteomics and Clinical data; Analysis of Protein sequence, structure, motion and		

Funding Source	Area	Project Name	Objective	Organisation	Status	Funding (Euros)	Duration
			data, Protein 3-D modelling and molecular graphics		evolution; Molecular interactions and Drug Design; Development of Computational Tools and Databases for Biologists.		
DBT	Bio-Informatics	Biotechnology Information System (BTIS) --- A National Bioinformatics Network	To establishe a high-speed and high-bandwidth network in the form of Virtual Public Network (VPN) named as BIOGRID INDIA in order to make effective use of the research information available.		Animal virus database developed and maintained by Center of university of Pune got recognized by CODATA, a Committee of International Council of Sciences on Data for science & technology and other international bodies.		
MoES		Ocean Observation Systems	Establishment and maintenance of Moored Data Buoy network in Indian seas, Real-time data collection of met-ocean parameters in Indian seas, Dissemination of data in real time	National Institute Of Ocean Technology, Chennai	Application using OceanBouy Data – Weather Prediction / Early Cyclone Warning, Ocean State Model Calibration, Climate Research, Satellite Data Validation, Port Development / Navigational Use		
MoES		National Geographical Information System (GIS)	GIS is very useful in managing disasters, natural resources and environment. Many programs and	Natural Resources Information System under			

Funding Source	Area	Project Name	Objective	Organisation	Status	Funding (Euros)	Duration
			institutions such as National Resources Information System (NRIS) and National Natural Resources Management System (NNRMS) of the Indian Space Research Organization, National Spatial Data Infrastructure (NSDI) and National Resources Data Management System (NRDMS) of Department of Science and Technology, and National Informatics Centre (NIC).	National, Natural Resources Management System (NNRMS), National Spatial Data Infrastructure (NSDI) of Department of Science and Technology (DST), Bhuvan Image Portal of Department of Space (DOS), National Informatics Centre (NIC), City-GISs (example Mumbai, Bangalore, Kanpur, Kolkata and many others).			
DST	Scientific Computing	Middleware for Online Remote Visualization of Weather Applications		C-DAC	Completed	18K	2010-12

Funding Source	Area	Project Name	Objective	Organisation	Status	Funding (Euros)	Duration
DST	Supercomputing	Coupled Climate Models on Grids		C-DAC	Completed	57K	2007-10
DST	Supercomputing	A Checkpointing Infrastructure for Parallel Scientific Applications on Computational Grids		C-DAC	Completed	33K	2007-10
CSIR	Supercomputing	Mathematical Modelling and Computer Simulation	Ocean Modeling, Solid Earth Modeling, Climate and Environmental Modeling, Computational Industrial Mechanics Programme	Centre for Mathematical Modelling and Computer Simulation (C-MMACS)	Several projects have been funded including: Seismic Hazard and Risk Assessment based on Pattern Recognition; Shear Wave Velocity Structure in Delhi City Using Microtremor Arrays; Crustal and mantle structure along the east-west corridor; Advanced Mathematical Modelling and Artificial Intelligence System in the Analysis of Geophysical Time Series		
CSIR	Real Time System Software	Electronics Engineering	Electronics System, Electron Tube, Semiconductors	Central Electronics Engineering Research Institute (CEERI)	Several projects have been funded including: Development of Novel Sensor System for application in Iron; Modular		

Funding Source	Area	Project Name	Objective	Organisation	Status	Funding (Euros)	Duration
					Reconfigurable Micro-manufacturing System; Development of signal conditioning circuitry/platform and development of mixed-signal sub-system blocks for sensor applications; Image Processing based smart system for human gesture identification; Development of sensor level reconfiguration technique for reconfigurable computing system.		

Table 2: Indian Government funded projects related to Computing Systems

5 Key actors in India Government funded projects

Indian actors that receive government funding for ICT research and development in India are far fewer compared to the number of actors involved in EU funded research. Indian Government funding for ICT research is provided only to research institutes, government supported agencies and universities and no industry participation in government funding occurs. The key actors that participate in Indian Government funded research are the following:

- Centre for Development of Advanced Computing (C-DAC) – in multiple locations
- Indian Institute of Science (IISc)
- Indian Institutes of Technologies (IIT) – in multiple locations
- Grid Applications Research Laboratory (GARL)
- Dhirubhai Ambani Institute of Information and Communication Technology (DA-IICT)
- Center for Soft Computing Research
- NITT Tiruchirappalli

Each of these actors is described below and accompanying each description is a sample listing of funded ICT related projects, along with websites links to further project information when these are available.

The sample projects listed are not restricted to those purely addressing Computing Systems topics as having an understanding of the scope of projects addressed by each actor provides a useful perspective on the research work undertaken, and the positioning of Computing Systems-specific research activities within each organisation.

5.1 Centre for Development of Advanced Computing (C-DAC)

Centre for Development of Advanced Computing (C-DAC) is the premier R&D organization of the Department of Information Technology (DIT), Ministry of Communications & Information Technology (MCIT) for carrying out R&D in IT, Electronics and associated areas. Â Different areas of C-DAC, had originated at different times, many of which came out as a result of identification of opportunities.

- The setting up of C-DAC in 1988 itself was to build Supercomputers in context of denial of import of Supercomputers by USA. Since then C-DAC has been undertaking the building of multiple generations of Supercomputer starting from PARAM with 1 GF in 1988.
- Almost at the same time, C-DAC started building Indian Language Computing Solutions with setting up of GIST group (Graphics and Intelligence based Script Technology); National Centre for Software Technology (NCST) set up in 1985 had also initiated work in Indian Language Computing around the same period.
- Electronic Research and Development Centre of India (ER&DCI), with various constituents starting as adjunct entities of various State Electronic Corporations, had been brought under the hold of Department of Electronics and Telecommunications

(now DIT) in around 1988. They were focusing on various aspects of applied electronics, technology and applications.

- With the passage of time as a result of creative echo system that got set up in C-DAC, more areas such as Health Informatics, etc., were created; while right from the beginning the focus of NCST was on Software Technologies; similarly C-DAC started its education & training activities in 1994 as a spin-off with the passage of time, it grew to a large efforts to meet the growing needs of Indian Industry for finishing schools.

C-DAC has today emerged as a premier third party R&D organization in IT&E (Information Technologies and Electronics) in India working on strengthening national technological capabilities in the context of global developments in the field and responding to change in the market needs in selected foundation areas. In that process, CDAC represents a unique facet working in close junction with DIT to realize national policy and pragmatic interventions and initiatives in Information Technology. As an institution for high-end Research and Development (R&D), C-DAC has been at the forefront of the Information Technology (IT) revolution, constantly building capacities in emerging/enabling technologies and innovating and leveraging its expertise, calibre, skill sets to develop and deploy IT products and solutions for different sectors of the economy, as per the mandate of its parent, the Department of Information Technology, Ministry of Communications and Information Technology, Government of India and other stakeholders including funding agencies, collaborators, users and the market-place.

Location	Sample Projects	Further Details	Funding Source
CDAC - Bangalore	Design and development of a dynamic Firewall solution.	http://202.141.136.153/cens/r&d.php	DIT
	Design and Development of Security Assessment System for Grid Environments		
	PAX- Insider Attack Detection for preventing Data exfiltration		
	Design and Development of a Hardware based Network Intrusion Prevention System		
	Development of an Adaptive Firewall System for grid environment		
	RUDRAA-New devised mechanism for signature formulation		
	Design and Development of an Enterprise wide Intrusion Detection System		
	Development of an Adaptive Intrusion Detection, Analysis & Response System		
	Research and Development in Network Measurements and QoS to build Self-Managed Network Solution		

Location	Sample Projects	Further Details	Funding Source
	Establishment Of Nationwide Quality Of Service Network Test bed Project (Indian QoS NETwork- IQNET)		
	Development of Multi-Factor Authentication System (Core R&D)		
	CONESIS – Concept Extraction in Social Information Systems (Core R&D)		
	National Grid Computing Initiative –Grid technology services for Operational Phase of GARUDA		
CDAC - Mumbai	EDGE - Enterprise wiDe self manaGed network solution	http://www.cdacmumbai.in/index.php/research_and_publications/projects/edge_enterprise_wide_self_managed_network_solution	DIT
	Implementation of National eGovernance Service Delivery Gateway (NSDG)	http://www.nsdg.gov.in/administration/	
	Research & Development in Network measurement to build and QOS Self Managed Network Solution	http://www.cdacmumbai.in/index.php/cdacmumbai/research_and_publications/projects	
	Enhancing accessibility for FOSS Desktops	http://www.cdacmumbai.in/index.php/research_and_publications/projects/enhancing_accessibility_for_foss_desktops	
	Establishment of a State Service Delivery Gateway (SSDG)	http://www.cdacmumbai.in/index.php/cdacmumbai/research_and_publications/projects	
	Decision Support for Automated Refractoring	http://www.cdacmumbai.in/index.php/research_and_publications/projects/decision_support_for_automated_refactoring	
	Architecture Framework for development of e-Governance Systems Project	http://www.cdacmumbai.in/index.php/research_and_publications/research_groups/software_engineering/r_d_projects/cffes	
	C-DAC eForm Engine Project	http://www.cdacmumbai.in/index.php/research_	

Location	Sample Projects	Further Details	Funding Source
		and_publications/research_groups/software_engineering/r_d_projects/cffes	
CDAC - Hyderabad	Wireless Sensor Network Integrated Development Environment (WSNIDE)	http://cdachyd.in/research-development/wsnide	DIT
	Smart PARKing (SPARK)	http://cdachyd.in/research-development/smart-parking/	
	U-Agri	http://cdachyd.in/research-development/u-agri/	
	Ubicomp	http://www.ubicomp.in/	
	EnSafe-Design and Development of a Security Framework for Ubiquitous Applications addressing Security	http://cdachyd.in/products/ensafe-1/ensafe-projects/?searchterm=projects	
CDAC - Pune	GARUDA	http://cdaccloud.com/cdaccloud/content/projects	DIT
	Development of Web GIS-enabled Road Information Management and Monitoring System for Orissa State	http://pune.cdac.in/index.aspx	
	Himalayan Glacier Inventory Mapping	http://pune.cdac.in/index.aspx	
	PARAMNet-II	http://pune.cdac.in/html/htdg/paramnet2.aspx	
	Fast ethernet switch	http://pune.cdac.in/html/htdg/products/fastethr.aspx	
	PCI based FDDI Adapter	http://pune.cdac.in/html/htdg/products/pciadapt.aspx	
	Sbus based Digital Data Acquisition Card	http://pune.cdac.in/html/htdg/products/sbus2.aspx	
	PCI based Digital Data Acquisition Card	http://pune.cdac.in/html/htdg/products/pci2.aspx	
	MEGH SUSHRUT (MS) – An ERP Solution for Health Delivery in SaaS Model using Garuda Network as the Computing Cloud	http://www.cdac.in/html/north-east/ongoing_proj/ms.aspx	

Location	Sample Projects	Further Details	Funding Source
	Grid Connected Solar Photovoltaic Power Plant for Deployment in North-East	http://www.cdac.in/html/north-east/ongoing_proj/grid.aspx	
	Comprehensive Spatial Decision Support System for Forest Management (Bodoland Territory)	http://www.cdac.in/html/north-east/ongoing_proj/bodoland_territory.aspx	
	Near - Real Time Flood Monitoring in Brahmaputra Valley using Microwave Remote Sensing	http://www.cdac.in/html/north-east/ongoing_proj/flood_monitoring.aspx	
	PARAM Anant	http://pune.cdac.in/html/npsf/anant/anantp.aspx	
CDAC - Noida	Browser Based Open Standard Inter-operable Set Top Box (STB)	http://www.cdacnoida.in/UC/STB.asp	DIT
	Design & Development of UHF RFID Reader	http://www.cdacnoida.in/UC/UHF_RFID.asp	
	RFID based Parcel Tracking System	http://www.cdacnoida.in/UC/RFID_Tracking.asp	
	RFID based Library management system	http://www.cdacnoida.in/UC/Library_management.asp	
	RFID based People Management System	http://www.cdacnoida.in/UC/RFID_Mgt.asp	
	OFDMA based Wireless Broadband System for Rural Connectivity	http://www.cdacnoida.in/UC/embedded_products.asp	
	Solar Powered Grain Moisture Measurement System	http://www.cdacnoida.in/UC/embedded_products.asp	
	Solar Powered Uninterrupted Power Supply	http://www.cdacnoida.in/UC/embedded_products.asp	
	Decision Support system for District Planning	http://www.cdacnoida.in/eGovernance/e_gov.asp	
	Online Activity Registrations for Municipal Corperation of Delhi (MCD)	http://www.cdacnoida.in/eGovernance/e_gov.asp	
	Project Parivartan for Indian Patent Office	http://www.cdacnoida.i	

Location	Sample Projects	Further Details	Funding Source
		n/eGovernance/e_gov.asp	
	Land Management Information System for Delhi Development Authority (DDA)	http://www.cdacnoida.in/eGovernance/e_gov.asp	
	Employee Information System (EIS) for MCD	http://www.cdacnoida.in/eGovernance/e_gov.asp	
	Security Management Information System (SMIS) for Indian Railways	http://www.cdacnoida.in/eGovernance/e_gov.asp	
	Personnel Management Information System (PMIS) for Indian Railways	http://www.cdacnoida.in/eGovernance/e_gov.asp	
	Land Information System (e-Governance for Gautam Budh Nagar)	http://www.cdacnoida.in/eGovernance/e_gov.asp	
	Constituency Management System (CMS) developed for District Muzaffarnagar	http://www.cdacnoida.in/eGovernance/e_gov.asp	

Table 3: Sample research projects at CDAC locations

5.2 Indian Institute of Science (IISc)

The Indian Institute of Science (IISC) was started in 1909 through the pioneering vision of J.N. Tata. Since then, it has grown into a premier institution of research and advanced instruction, with more than 2000 active researchers working in almost all frontier areas of science and technology. IISC is an institute of higher learning and is constantly in pursuit of excellence. It is one of the oldest and finest centres of its kind in India, and has a very high international standing in the academic world as well.

Besides formal education and research, the Institute has been playing an active part in offering short-term courses to scientists and technologists in service. The Continuing Education Programme covers a wide range of topics and over 1500 working scientists and engineers go through such courses every year.

In keeping with its aims and objects, the Institute has organised a Centre for Scientific and Industrial Consultancy through which the know-how generated in the Institute percolates to industries via industry-sponsored projects.

The Centre for Electronics Design and Technology (CEDT) was established in 1974, with the joint support of the then Department of Electronics (DoE), Ministry of Education, University

Grants Commission and Swiss Agency for Development and Co-operation under the Technical and Scientific Co-operation Agreement.

The expertise of CEDT spans communication technologies and networks: IPv4/IPv6 Internet applications, Wireless Adhoc and Sensor Networks; 3G Cellular Systems; Emerging Wireless Standards; Internet Pricing, security and QoS.

IISc also hosts the Supercomputer Education and Research Centre (SERC), which focuses on advanced research and education in various aspects of Computer Systems. The centre provides a state-of-the-art computing environment comparable to top Computing Centres around the world and is engaged in cutting-edge research programs in areas relating to high-performance systems and applications. The research focus of SERC can be broadly classified into three areas, namely Computer Systems, Computational Science and Bioinformatics. The active research areas pursued by SERC related to Computing Systems are the following:

- System on Chip and Embedded Processor Architectures
- Computer Architecture
- Compiler Optimization
- Database Systems
- Graphics and Visualization
- Grid Computing and High Performance Computing
- Multimedia Systems and Information Security
- Parallel Numerical Algorithms

SERC has a faculty of 24, with 22 Doctorate level and 55 Masters level students involved in several sponsored research projects in collaboration with government agencies and industrial organisations.

Sample Projects	Further Details	Funding Source
Parallel distributed file system for message passing architecture	http://www.serc.iisc.ernet.in/researchnprojects/SponsoredResearchProjects.html	DST
A checkpointing infrastructure for parallel scientific applications on computational grids		
Language database development for example based machine translation		
Hardware software co-design of network switches		
Setting up internet/firewall servers for the Distributed Information Centres under the Bio-Technology Information Systems programme of the Dept of Bio-Technology		DBT

Table 4: Sample research projects at IISc

5.3 Indian Institutes of Technologies (IIT)

The Indian Institutes of Technology (IITs) are a group of autonomous engineering and technology-oriented institutes of higher education. The IITs are governed by the Institutes of Technology Act in 1961, which declared them as “institutions of national importance”, and lays down their powers, duties, framework for governance, etc. They were created to train scientists and engineers, with the aim of developing a skilled workforce to support the economic and social development of India. IITs are listed as societies under the Indian Societies Registration Act.

The seven institutes which comprise the IIT grouping, in order of establishment are as follows:

- IIT Kharagpur (1950)
- IIT Bombay in Mumbai (1958)
- IIT Madras in Chennai (1959)
- IIT Kanpur in Kanpur (1959)
- IIT Delhi in New Delhi (1961)
- IIT Guwahati (1994)
- IIT Roorkee (2001)

A further nine institutes were also established by the Indian government in 2011; however these newer organisations are in various stages of consolidation and development.

Three of the founding seven institutes receive India government funding for carrying out research and development project addressing topics in Computing Systems. It’s interesting to note that all three were established with substantial support from outside India. A summary of each of these Institutes is provided in the following.

IIT Madras

The Indian Institute of Technology Madras is an engineering and technology school in Chennai (formerly Madras) in southern India. Founded in 1959 with technical and financial assistance from the government of the former West Germany, it is third the largest amongst the Indian Institutes of Technology established to provide education and research facilities in engineering and technology.

IIT Madras is a residential institute that occupies a 2.5 km² (620 acres) and has nearly 360 faculty, 6,000 students and 1,250 administrative and supporting staff. The Department of Computer Science addresses research in the areas of:

- Programming Languages, Compilers and Software Engineering
- Hardware Systems
- Networks and Distributed Systems
- Human Computer Interaction
- Intelligent Systems and Knowledge Engineering

The Department has a student body numbering about 400. Over 60% are postgraduate, mostly supported by scholarships. Over 50 full-time engineers work on R&D projects.

IIT Kanpur

The Indian Institute of Technology Kanpur located in Uttar Pradesh, about 15 km north-west of the city of Kanpur in the Kalyanpur suburb. The institute was created with the assistance of a consortium of nine leading US research universities as part of the Kanpur Indo-American Programme. The Institute was the first in India to start Computer Science education with the initial "computer-related" courses starting in August 1963 and the Computer Science department remains highly regarded in India in terms of excellence in research and teaching in Computer Science and Engineering.

The Department of Computer Science and Engineering currently has a faculty of 22 and admits about 30 students every year in the Bachelors programme and 50 students in the Masters programme. The Department currently addresses research in the areas of:

- Computer and Internet Security
- Compilers and Programming Languages
- Natural Language Processing
- Networking
- Discovery, Learning, and Cognition

There are approximately 15 students registered in Ph.D. program at a time. There are two software engineers and two other staff attached to the laboratory facilities. There are also a number of research engineers working in various sponsored projects.

IIT Bombay

IIT Bombay was established in 1958 with assistance from UNESCO and with funds contributed by the Soviet Union. UNESCO agreed to provide equipment and technical experts mainly from the Soviet Union, while the Government of India accepted the responsibility for all other expenses including the cost of the building project and recurring expenses. The Computer Science and Engineering department is the largest Computer Science and Engineering department in India and addresses research projects in the following areas:

- Programming languages and Compilers
- Database and Information Systems and Data Mining
- Artificial Intelligence and Natural Language Processing
- Formal Methods
- Distributed Systems
- Computer Networks
- Computer Graphics, Computer Vision and Image Understanding

- Real-Time and Embedded Systems
- Formal Languages and Bio-inspired Computing

The Department consists of 36 faculty members, 80 PhD. students, 200 Masters level students, 170 undergraduates and 25 staff members.

Location	Sample Projects	Further Details	Funding Source
IIT - Chennai	Redesign of the Linux Kernel in Service-oriented Architecture (SOA)	http://dos.iitm.ac.in/projects/DIT/	DIT
	Minimalistic Object Oriented Linux (MOOL)	http://dos.iitm.ac.in/projects/MOOL/	
	TOOLS for integration of software processors with Unified Reuse Artefacts	http://dos.iitm.ac.in/projects/dst.html	DST
	Computing Power Grids on Middleware	http://dos.iitm.ac.in/projects/dstnew.html	
IIT - Bombay	Development of algorithms for modelling and controller design for dynamical systems	http://www.ee.iitb.ac.in/~ccgroup/	
IIT - Kanpur	Design and Development of a Gigabit Network Monitoring Tool	http://www.cse.iitk.ac.in/research/projects.html	DIT
	PickPacket - A Generalized Network Monitoring Tool	http://www.security.iitk.ac.in/index.php?page=contents/projects/pickpacket/pickpacket	
	TIED, LibsafePlus: The complete buffer overflow solution	http://www.security.iitk.ac.in/index.php?page=contents/projects/tied_libsafe/tied_libsafeplus	

Table 5: Sample research projects at IITs

5.4 Grid Applications Research Laboratory (GARL)

Grid Applications Research Laboratory (GARL) was started in 2004 by the Supercomputer Education and Research Centre at Indian Institute of Science (IISc), Bangalore. The lab deals with High Performance Computing systems and applications and aims to become an internationally competent laboratory carrying pioneering research work in the area of large scale systems and applications.

The applications areas addressed by GARL focuses are parallel applications including multi-physics applications, adaptive mesh refinement, n-body simulations, and other large-scale and long-running applications. The systems areas emphasise dynamic systems including GPUs, state-of-the-art supercomputers and grid systems. Current research areas include the following:

- Application optimization
- Fault tolerance
- Middleware for batch systems
- Performance modelling, scheduling & rescheduling

The Laboratory employs a staff of approximately 15 people with various Masters and PhD students from the IISc contributing to research projects.

Sample Projects	Further Details	Funding Source
Middleware for Online Remote Visualization of Weather Applications	http://garl.serc.iisc.ernet.in/projects/	CDAC
Coupled Climate Models on Grids	http://garl.serc.iisc.ernet.in/projects/	DIT
A Checkpointing Infrastructure for Parallel Scientific Applications on Computational Grids	http://garl.serc.iisc.ernet.in/projects/	DST
Development of Grid Computing	http://garl.serc.iisc.ernet.in/projects/	IISc

Table 6: Sample research projects at GARL

5.5 Dhirubhai Ambani Institute of Information and Communication Technology (DA-IICT)

Dhirubhai Ambani Institute of Information and Communication Technology (DA-IICT), is a private technological institute located in Gandhinagar, Gujarat, India. DA-IICT began in August 2001 with an intake of 240 undergraduate students for its Bachelor of Technology program in Information and Communication Technology. Today the Institute has over 900 undergraduate students and 200 postgraduate students, who are selected on the basis of merit. Students who are admitted into the Ph.D. programme receive a generous stipend, which is amongst the highest in the country.

The Institute has departments addressing education and research in Computer Science, Electronics and Communication, Information Technology and ICT for Agriculture and Rural Development. The Institute carries out research projects in the following areas:

- Communication and Signal Processing
- Distributed & Service-Oriented Computing
- ICT in Agriculture & Rural Development
- Natural Information Processing
- Networks & Security

- Pattern Recognition & Image Processing
- Sensor Networks
- VLSI
- Wireless communication

DA-IICT has close ties with the Indian industrial group Reliance Communications whose late founder established the Institute. Many of the Institute's external governing board members are currently from Reliance Communications.

Sample Projects	Further Details	Funding Source
Reconfigurable embedded system for motor control	http://intranet.daiict.ac.in/~ranjan/research/projects.htm	DST

Table 7: Sample research projects at DA-IICT

5.6 Center for Soft Computing Research, Indian Statistical Institute

The Center has been set up at the Indian Statistical Institute (ISI), Kolkata in recognition by the Department of Science and Technology of the Government of India of the contributions and achievements in the area of soft computing and machine intelligence. The Center is aimed at conducting research both theoretical and applied, of international standard, in the fields of soft computing and was formally inaugurated in 2005.

The research topics addressed by the Center include:

- Machine learning
- Pattern recognition
- Data mining
- Web intelligence
- Image processing and analysis
- Neural, evolutionary and swarm computing
- Bioinformatics
- Granular computing
- Cognitive vision

The Center currently has 20 Investigators and Researchers carrying out projects and also supervises projects carried out by other researchers and Indian universities and institutes that are funded by the Indian Government's Department of Science and Technology.

Sample Projects	Further Details	Funding Source
Soft Computing Techniques to solve Routing and Wavelength Assignment (RWA) Problem in Optimal Networks	http://www.isical.ac.in/~scc/	DIT
ANN-GA and ANFIS Models Development for Flood Forecasting with Multiple Inflows in Break River Network		
Fuzzy Techniques for Opinion Mining in a Social Networking Environment		
Development of ANN and GA Aided Engineered Woven Structures for Improved Solar Ultraviolet Radiation Protection		
Statistical, Structural and Soft Computing based Techniques for Pattern Recognition: Theory, Algorithms and Applications to Bioinformatics		

Table 8: Sample research projects at the Center for Soft Computing Research

5.7 NITT Tiruchirappalli

The National Institute of Technology Tiruchirappalli, situated in Tamil Nadu was started as a joint and co-operative venture of the Government of India and the Government of Tamil Nadu in 1964 with a view to catering to the needs of man-power in technology for the country and was granted University Status in 2003 and renamed as National Institute of Technology. The institution offers Under Graduate Courses in ten branches and Post Graduate Courses in twenty-one disciplines of Science, Engineering & Technology besides Ph.D. in all the departments.

The Department Current research projects are being carried out in the areas of:

- Networks
- Data base management systems
- Operating systems
- Image processing

The Department has a faculty of 15 approximately 200 undergraduate students and 30 graduate level students.

Sample Projects	Further Details	Funding Source
Optimization Techniques for the FGPA implementation of high speed digital communication blocks for software defined radio	http://www.nitt.edu/home/icsr/sr/	DST
Online control of multivariable process using soft		

Sample Projects	Further Details	Funding Source
computing		

Table 9: Sample research projects at NITT Tiruchirappalli

5.8 Geographic distribution of actors

Figure 5 shows the geographic distribution by region of the key actors that participate in government funding Computing Systems research projects in India.

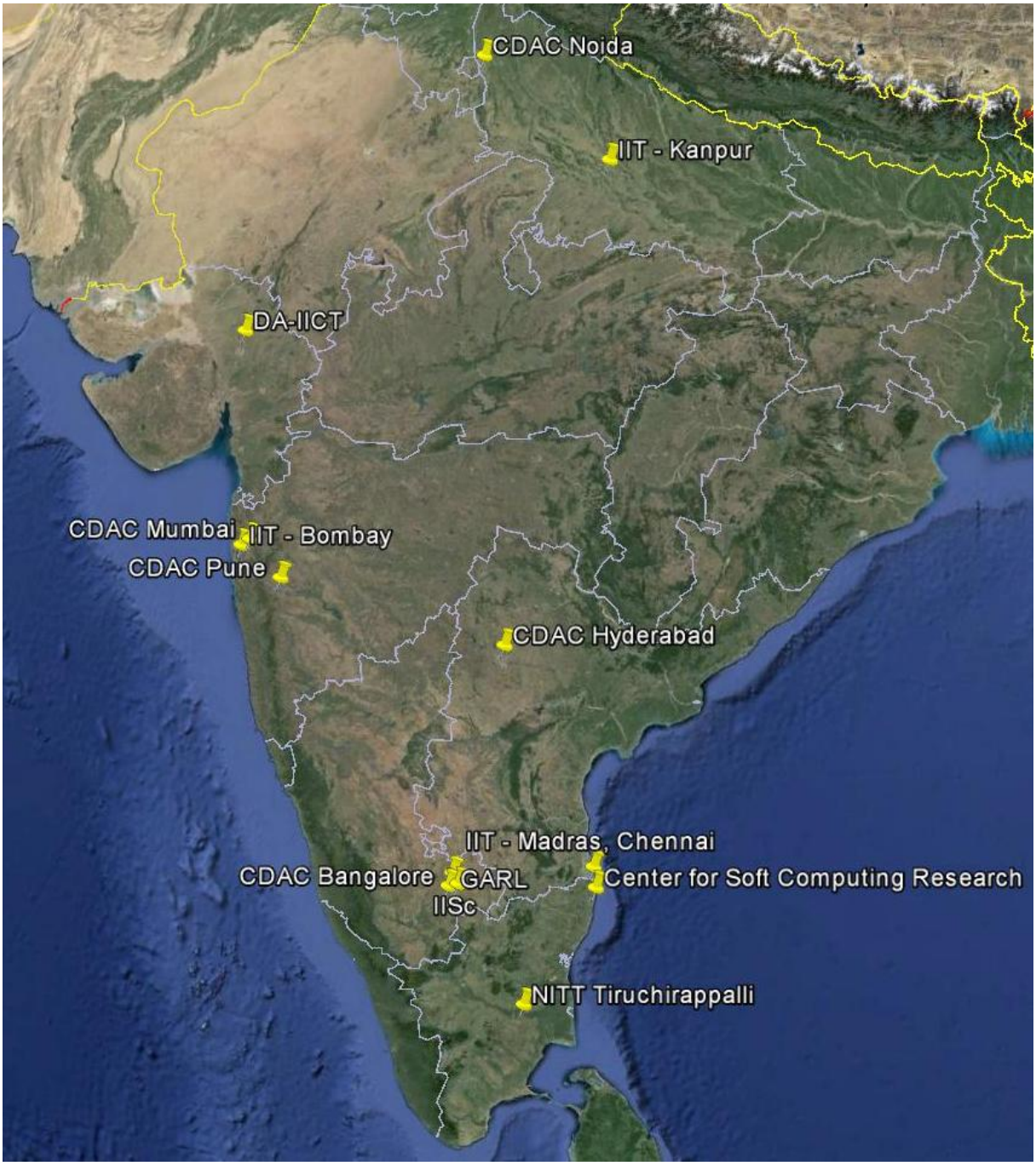

Figure 5: Geographic locations of Indian actors involved in Computing Systems projects

Indian actors are distributed geographically around the country with a slight concentration in Bangalore where there are facilities for IISc, CDAC and the Grid Applications Research Laboratory (GARL).

6 EU funded projects related to Indian Government funded projects

6.1 Overview

The EU-INCOOP partners see an important opportunity to increase collaboration between EU and India Government funded projects that are addressing similar topics. As of the date of this report, there have been no Indian organisations involved in EU funded Computing Systems research and development projects[1] in FP7 (2007-2013), even though the EC programmes provides financial support for Indian organisations to participate. The reasons behind this and the actions needed to increase participation of Indian organisations in future EU funded research will be addressed in upcoming deliverables of the EU-INCOOP project.

A more immediate opportunity exists for collaboration between the EU and India research organisations related to ongoing or recently completed projects. This section of the document identifies the EU funded projects involved in technology research topics that are related to projects funded by the Indian Government, based on an analysis of both EU and Indian government funded projects.

The listing of Indian government projects that were considered are found in Section 4 of this document, while the listing of EU funded projects are available from the European Commission website with information concerning the FP7 ICT Computing Systems objective at: http://cordis.europa.eu/fp7/ict/computing/fp7-projects_en.html. As noted above, the scope of the projects that were investigated were those in operation during the FP7 timeframe (2007-2013) or still ongoing.

6.2 Methodology

The methodology that was used to identify EU funded projects related to Indian funded projects started with an initial structuring of the EU projects provided by the European Commission as shown in Figure 6.

[1] A few Indian organisations have been in involved in Coordination Action projects in Computing Systems, but not in technology development projects.

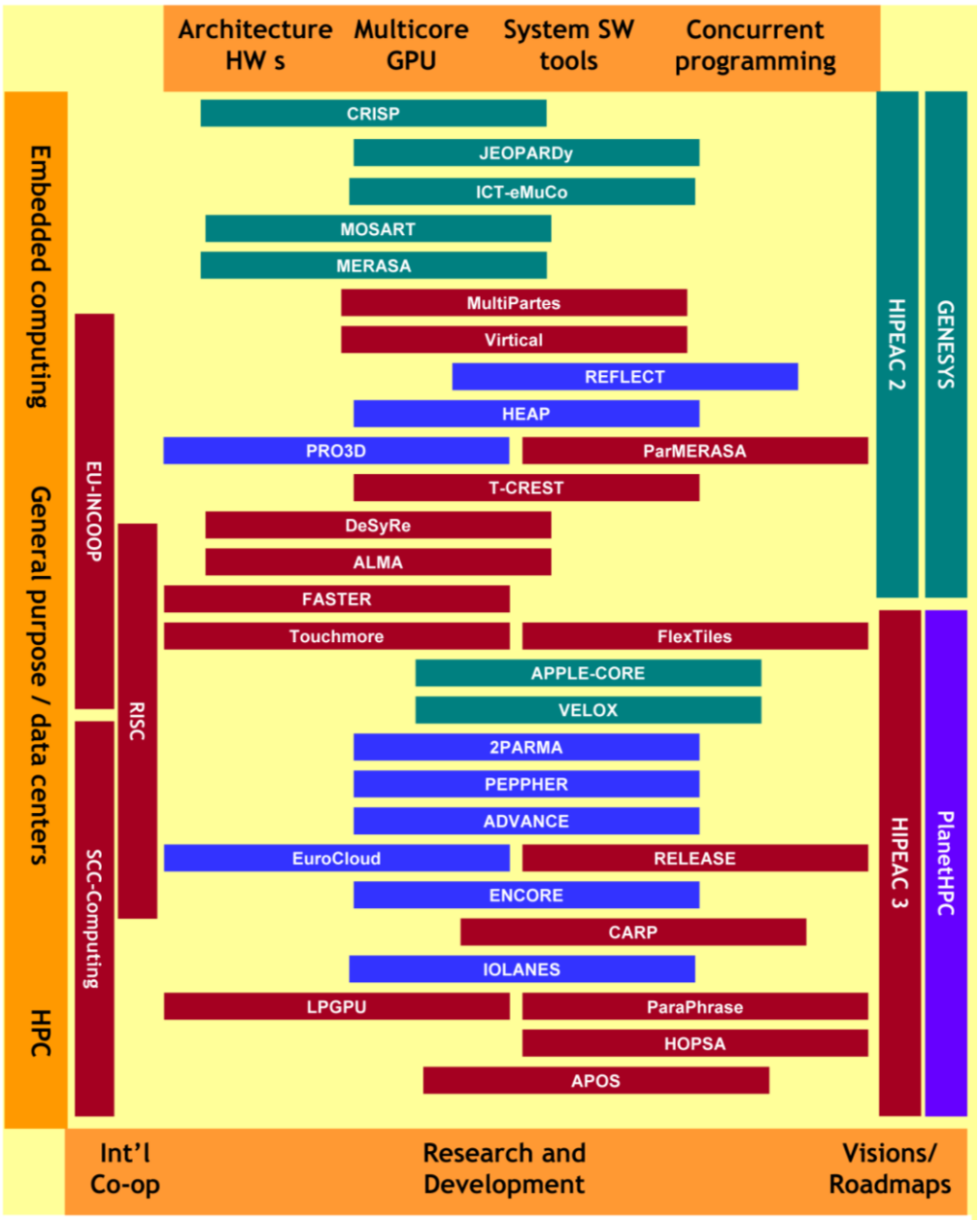

Figure 6: Overview of FP7 Research on Computing Systems[2]

The European Commission identified the following four high level categories of technology development being undertaken in the projects that were funded:

- Architecture and Hardware
- Multicore and GPU
- System Software and Tools
- Concurrent Programming

This categorisation provided a good first grouping, but was not quite granular enough to be used as selection criteria for identifying common technology interests at the project level

[2] European Commission figure from: http://cordis.europa.eu/fp7/ict/computing/documents/overview-fp7-projects.pdf

between India and the EU. A further refinement was made by carrying out a review of all 33 research and development projects funded under the EU FP7 Computing Systems programme. The analysis resulted in eight categories of development topics being identified. These topics represented the major research and development areas amongst the EU projects at a level that could be used for evaluating and comparing project topics:

- Multicore
- Virtualisation
- Parallelisation
- Platform and Hardware
- Performance Analysis
- Predictability
- Reconfigurability
- Composability

Most of the above categories need little explanation in this document, however some terms that may be less familiar are described as follows:

- Predictability – technologies and tools associated with hard real-time requirements where timing or use of system resources must be guaranteed (e.g. EU projects ParMERASA and T-CREST).
- Reconfigurability – technologies that enable reconfiguration of processing and system resources to meet specific application and performance requirements (e.g. EU projects Paraphrase, 2Parma and CRISP).
- Composability – technologies to allow systems to be comprised of smaller components that can be assembled and restructured with specific characteristics and according to specific application or system requirements (e.g. EU projects Peppher and PRO3D).

The final part of the methodology was to review and classify each of the Indian funded research projects to determine those projects that were addressing technologies in one or more of the eight categories being addressed by the EU funded projects.

A complicating factor in carrying out the review of Indian projects was the difference in the scope of the projects that are funded in India. The EU research projects typically are addressing technologies with wide impact as demonstrated by the fact they often target more than one application domain (i.e. Aerospace, Automotive, Medical, etc.). There are similar projects in India, but there are also funded projects that are developing Computing Systems technology to address one particular target application (i.e. mathematical modelling of proteins). This required additional investigation to distinguish between projects developing new Computing Systems technologies and those that are applying existing technologies in novel ways to address specific applications.

Another aspect to the analysis was centred on opportunities for further collaboration between the EU and India. In some cases it was clear the Indian funded project was focusing on applied Computing Systems technologies rather than research and development of new technologies. These Indian projects were still considered in the analysis since in many cases

it was viewed that the Indian project would likely benefit from use and exploitation of EU funded project technologies addressing similar challenges. For example, an applied technology project in India might prove to be an excellent test bed or validation site for results from a related EU research project.

6.3 Identified EU projects

The methodology described in Section 6.2 for analysing projects resulted in two research categories being most prevalent amongst India funded projects:

- Multicore
- Parallelisation

The prevalence of Multicore and Parallelisation related research and development were almost equal amongst Indian projects, with Performance Analysis also being prevalent, but to a slightly lesser level than the first two.

The EU-INCOOP project has used this result from analysing India funded projects to identify EU funded projects where at least two of the Indian prevalent research topics of Multicore, Parallelisation or Performance Analysis are being addressed. These EU funded projects are shown in Table 10 and represent the EU projects funded by the European Commission that are most related to India funded projects.

The listing in the table is ordered according to the European Commission's Calls for Proposals. The Call timing is important as it indicates which EU projects are likely to still be in operation:

- Call 7 Projects – typically are in the early phases of development with many of these projects having started in the latter part of 2011.
- Call 4 Projects – typically mature and well along in their development work with many nearing the end of their project.
- Call 1 Projects – these will usually be completed projects but will have completed recently enough that project partner contacts are likely to still be the same.

Additional information about partners and contacts for the selected EU projects in Table 10, can be found by using the European Commission's project search facility at: http://cordis.europa.eu/fp7/ict/projects/home_en.html, as well as by following the links to the website provided for each project.

Project Number	Acronym	EC Call	Title	Website
277481	APOS-EU	7	Application Performance Optimisation and Scalability	www.apos-project.eu
288570	PARAPHRASE	7	Parallel Patterns for Adaptive Heterogeneous Multicore Systems	www.paraphrase-ict.eu
287519	ParMERASA	7	Multi-Core Execution of Parallelised Hard Real-Time Applications	www.parmerasa.eu

Project Number	Acronym	EC Call	Title	Website
			Supporting Analysability	
287510	RELEASE	7	A high-Level Paradigm for Reliable Large-scale Server Software	www.release-project.eu
288166	TOUCHMORE	7	Automatic Customizable Tool-chain for Heterogeneous Multicore Platform Software Development	www.touchmore-project.eu
248647	ENCORE	4	ENabling technologies for a programmable many-CORE	www.encore-project.eu
247615	HEAP	4	A Highly Efficient Adaptive multi-Processor framework	www.fp7-heap.eu
215216	APPLE-CORE	1	Architecture Paradigms and Programming Languages for Efficient programming of multiple CORES	www.apple-core.info
216682	JEOPARD	1	Java Environment for Parallel Realtime Development	www.jeopard.org
215244	MOSART	1	Mapping Optimisation for Scalable multi-core ARchiTecture	www.mosart-project.org
216852	VELOX	1	An Integrated Approach to Transactional Memory on Multi- and Many-core Computers	www.velox-project.eu

Table 10: EU funded projects closely related to India funded projects

A description of each of the projects identified along with the project coordinator and contact information and partners involved in the project is provided below.

6.3.1 APOS-EU

The objective of APOS-EU is to develop optimised versions of scientific and industrial codes which are scalable and portable across heterogeneous and homogeneous architectures. Codes will be chosen from the areas of seismic processing, magneto-hydrodynamics, percolation, molecular modelling and CFD. Scalability to thousands of cores will be a principal goal of the work. In parallel with the development of the codes, prototype tools, starting from the current state of the art, will be interactively developed, deployed and refined.

The proposal falls within Part C of the call Objective ICT-2009.10.2 EU-Russia Research and Development Cooperation. This proposal is a small, but important step on the road to innovative, advanced simulations and tools to support their development. Real-world applications will be used to test and evaluate methodologies for developing massively parallel, highly scalable applications and for testing relevant tools. This will provide an important reference to code owners both ISVs and those with in-house codes. It will provide important feedback to tool developers on the requirements of porting real applications to the new generations of machine. The successful outcome of the project will constitute an

important advance in the state of the art and will have immediate industrial and economic impact.

The work in APOS-EU will be complemented by that in the Russian proposal APOS-RU which addresses two important application areas namely high-resolution 3-D seismic processing and atomic simulation codes based on many-body interatomic potentials. Both these areas create opportunities for common work between the EU and Russian consortia on the development of algorithms and on the use and development of tools for parallelisation.

Project Coordinator

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Website: www.apos-project.eu

Project Partners

UNIWERSYTET WARSZAWSKI	POLAND
UNIVERSITAET STUTTGART	GERMANY
TOTAL	FRANCE
CAPS ENTREPRISE	FRANCE

6.3.2 PARAPHRASE

A revolution is happening in computer hardware. After three decades during which microprocessor speeds increased almost 4000 times, we are starting to hit long-predicted physical limits on the speed of a single processor. Recent computers instead use two, four or even twelve processor cores working together ''in parallel', giving peak performance that is equivalent to a 5GHz, 10GHz or even 30GHz single processor, but at a fraction of the projected energy usage. There have even been experimental 48-core ''single cloud computer' chips giving peak performance that would exceed that of a 100GHz single processor. The effective exploitation of such high performance is essential to support modern demands for computing power in the home, in industry and in the economy at large. Combining this with low energy usage is crucial if the performance is to be delivered at a reasonable financial and environmental cost.

Future designs will harness even greater numbers of processor cores, perhaps in the thousands or millions, and perhaps with widely varying speeds and capabilities. These will be combined with advanced graphics processor units and other specialist units to give further performance and energy gains. In this way we will be able to meet society's future needs for computing power.

While there are already significant challenges in building computers, such as those described above, from heterogeneous processor and other computing units, there are even greater challenges in building parallel software that can use them effectively. In order to do this, we must produce software that is easy to write but that still allows the hardware to be used effectively.

The key innovation of the ParaPhrase project is exactly to produce such software that is easy to write using the hardware more effectively with the goal of speeding up processing by at least one order of magnitude over sequential execution on real near-term multicore architectures for the use cases and systems that will be considered in the project.

ParaPhrase will build on a (multi-level) model of parallelism, where implementations of parallel programs are expressed in terms of interacting components. By expressing parallelism in terms of high-level parallel patterns that have alternative parallel implementations, we will be able to redeploy/refactor parallel components to dynamically match the available hardware resources.

One large scale company (MELLANOX), one SME (ERLANG SOLUTIONS) and an Austrian software competence centre (SCCH) with strong links to industry will exploit the project results in a commercial context. ParaPhrase will strengthen their respective market position and competitiveness and give a manifold return on investment. The six academic partners will use the gained knowledge to enrich their teaching activities and to reinforce their prestige in the scientific community. European citizens will benefit from less power-consuming computers.

Project Coordinator

UNIVERSITY OF ST ANDREWS	UNITED KINGDOM

Contact: www.paraphrase-ict.eu/contact-info (project website form)

Website: www.paraphrase-ict.eu

Project Partners

MELLANOX TECHNOLOGIES	ISRAEL
SOFTWARE COMPETENCE CENTER HAGENBERG	AUSTRIA
UNIVERSITAET STUTTGART	GERMANY
UNIVERSITA DEGLI STUDI DI TORINO	ITALY
THE QUEEN'S UNIVERSITY OF BELFAST	UNITED KINGDOM
ERLANG SOLUTIONS LIMITED	UNITED KINGDOM
THE ROBERT GORDON UNIVERSITY	UNITED KINGDOM
UNIVERSITA DI PISA	ITALY

6.3.3 ParMERASA

Engineers who design hard real-time embedded systems express a need for several times the performance available today while keeping safety as major criterion. A breakthrough in performance is expected by parallelising hard real-time applications. parMERASA targets a timing analysable system of parallel hard real-time applications running on a scalable multi-core processor. Several new scientific and technical challenges will be tackled in the light of timing analysability: parallelisation techniques for industrial applications, operating system virtualisation and efficient synchronisation mechanisms, guarantee of worst-case execution times (WCET) of parallelised applications, verification and profiling tools, and scalable memory hierarchies together with I/O systems for multi-core processors.

The output of parMERASA will be at least an eightfold performance improvement of the WCET for parallelised legacy applications in avionics, automotive, and construction machinery domains in comparison to the original sequential versions. The execution platform, i.e. the parMERASA multi-core processor and system software, will provide temporal and spatial isolation between tasks and scale up to 64 cores. A software engineering approach will be taken targeting at least four parallel execution patterns that are analysable. Verification and profiling tools will be developed, and we aim to provide at least four recommendations to enhance both automotive and avionic standards.

parMERASA will impact new products for transportation systems and industrial applications. It will impact standards by introducing parallel execution and time predictability as key features. This will contribute to reinforce the EC position in the field of critical computing systems and yield an advantage for European industry in the highly competitive avionics, automotive, and construction machinery markets.

Project Coordinator

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Project Partners

RAPITA SYSTEMS	UNITED KINGDOM
BARCELONA SUPERCOMPUTING CENTER	SPAIN
BAUER MASCHINEN	GERMANY
UNIVERSITE PAUL SABATIER TOULOUSE III	FRANCE
HONEYWELL INTERNATIONAL	CZECH REPUBLIC
DENSO AUTOMOTIVE DEUTSCHLAND	GERMANY
TECHNISCHE UNIVERSITAET DORTMUND	GERMANY

6.3.4 RELEASE

The exponential growth in the number of cores requires radically new software development technologies. Many expect 100,000-core platforms to become commonplace, and the best predictions are that core failures on such an architecture will be common, perhaps one an hour. Hence we require programming models that are not only highly scalable but also reliable. The project aim is to scale the radical concurrency-oriented programming paradigm to build reliable general-purpose software, such as server-based systems, on massively parallel machines.

The trend-setting language we will use is Erlang/OTP which has concurrency and robustness designed in. Currently Erlang/OTP has inherently scalable computation and reliability models, but in practice scalability is constrained by aspects of the language and virtual machine. Moreover existing profiling & debugging tools don't scale. The RELEASE consortium is uniquely qualified to tackle these challenges and we propose to work at three levels: - evolving the Erlang virtual machine so that it can work effectively on large scale multicore

systems; - evolving the language to Scalable Distributed (SD) Erlang, and adapting the OTP framework to provide both constructs like locality control, and reusable coordination patterns to allow SD Erlang to effectively describe computations on large platforms, while preserving performance portability;- developing a scalable Erlang infrastructure to integrate multiple, heterogeneous clusters.

We will develop state of the art tools that allow programmers to understand the behaviour of massively parallel SD Erlang programs. We will demonstrate the effectiveness of the RELEASE approach using demonstrators and two large case studies on a Blue Gene. Erlang is a beacon language for distributed computing, influencing both other languages and actor libraries and frameworks. Hence we expect the project to make a strong and enduring impact on computing practice in the two decades.

Project Coordinator

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Project Partners

ELECTRICITE DE FRANCE	FRANCE
UPPSALA UNIVERSITET	SWEDEN
ERICSSON	SWEDEN
UNIVERSITY OF KENT	UNITED KINGDOM
ERLANG SOLUTIONS	UNITED KINGDOM
INSTITUTE OF COMMUNICATION AND COMPUTER SYSTEMS	GREECE

6.3.5 TOUCHMORE

Recent trends in embedded system architectures brought a rapid shift towards multicore, heterogeneous and reconfigurable platforms. This makes chip design enormously complex and imposes a large effort for the programmers to develop their applications. For this reason, new and more efficient tools for software development are needed to ensure software productivity and time to market of new applications. In particular, the automation of the software design process starting from high level models all-the-way down to a customized and implementation on specific architectures is a key factor to increase programmer productivity.

The TouchHMore project will develop software tools that facilitate energy efficient and robust software for Heterogeneous Multicore Systems (HeMCS) with the goal to reduce the time-to-market in the design of such systems by at least 15%, as well as the cost of software design through the automation process by 20%. In more detail, the center of the methodology is the high level modelling language (UML/SysML) that will be used to describe the target platform and application. High level modelling allows an architectural independent description of the application and for this reason it is prone to customization for different architectural templates. In TouchHMore, customization will be performed in an

automated way through automated generation of parallel code for multicore tiles and the required mechanisms to manage reconfigurable DSPs/accelerators. In addition, the ToucHMore tool-chain customization environment will focus on energy efficiency and robustness of the generated code, where the uncertainties due to fabrications of transistors in nanometer technologies will be hidden, thus mitigating their impact in terms of energy and performance. From a research perspective, ToucHMore is a pioneering project from the perspective of taking a pragmatic approach to bring variability issues into the software design flow. Together with the automatic tool chain customization strategy coupled with high level modelling, these contribution will give the European research on embedded software a leading position.

The project results will be commercially exploited by the SME ATEGO as a specialised software tool vendor and by the company AKHELA that is an IT services and Embedded Systems provider to large scale companies in areas such as automotive, avionics and consumer electronics. The project results will strengthen their position in their respective markets by enabling the production of products faster and more timely than the world wide competitors and it is expected that they will have a manifold return on their investment. The five research institutions will use the gained knowledge to enrich their teaching and research activities enabling them to stay at the forefront of technology and substantiating their prestige in the scientific community.

Project Coordinator

POLITECNICO DI TORINO	ITALY
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Website: www.touchmore-project.eu	

Project Partners

CSEM	SWITZERLAND
CEA	FRANCE
UNIVERSITY OF YORK	UNITED KINGDOM
ATEGO SYSTEMS	UNITED KINGDOM
ATEGO	FRANCE
UNIVERSITA DEGLI STUDI DI VERONA	ITALY
AKHELA	ITALY

6.3.6 ENCORE

Design complexity and power density implications stopped the trend towards faster single-core processors. The current trend is to double the core count every 18 months, leading to chips with 100+ cores in 10-15 years. Developing parallel applications to harness such multicores is the key challenge for scalable computing systems.

The ENCORE project aims at achieving a breakthrough on the usability, reliability, code portability, and performance scalability of such multicores. The project achieves this through three main contributions. First, by defining an easy to use parallel programming model that

offers code portability across several architectures. Second, by developing a runtime management system that will dynamically detect, manage, and exploit parallelism, data locality, and shared resources. And third, by providing adequate hardware support for the parallel programming and runtime environment that ensures scalability, performance, and cost-efficiency.

The technology will be developed and evaluated using multiple applications, provided by the partners, or industry-standard benchmarks, ranging from massively parallel high-performance computing codes, where performance and efficiency are paramount, to embedded parallel workloads with strong real-time and energy constraints. The project integrates all partners under a common runtime system running on real multicore platforms, a shared FPGA architecture prototype, and a large-scale software simulated architecture. Architecture features will be validated through implementation on ARM's detailed development infrastructure.

ENCORE takes a holistic approach to parallelization and programmability by analyzing the requirements of several relevant applications ranging from High Performance Computing to embedded multicore, by parallelizing these applications using the proposed programming model, by optimizing the runtime system for a range of parallel architectures, and by developing hardware support for the runtime system.

Project Coordinator

BARCELONA SUPERCOMPUTING CENTER	SPAIN

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Website: www.encore-project.eu

Project Partners

ARM	UNITED KINGDOM
ISRAEL INSTITUTE OF TECHNOLOGY	ISRAEL
FOUNDATION FOR RESEARCH AND TECHNOLOGY HELLAS	GREECE
TECHNISCHE UNIVERSITEIT DELFT	NETHERLANDS
KUNGLIGA TEKNISKA HOEGSKOLAN	SWEDEN

6.3.7 HEAP

Writing parallel code has traditionally been considered a difficult task, even when it is taken into account from the beginning. At the same time, while processor architecture tends to be relatively standard across applications within a domain, huge performance and power improvements can be achieved by tailoring the cache architecture, to the application at hand.

The HEAP project faces these challenges directly, by providing:

- An innovative toolset that helps software developers profile and parallelize an existing sequential implementation, by exploiting top-level pipeline-style parallelism.

- A highly configurable cache architecture that can be tailored to an application by using the same, or similar, profiling data as those that were used for parallelization, in order to fully exploit the available computing power.

We innovate in the first domain by using both pessimistic and optimistic estimates of the available parallelism, by refining those estimates using metric-driven verification techniques, and by supporting dynamic recovery of excessively optimistic parallelization.

We innovate in the second domain by treating cache coherence not as an immutable substrate, that is the burden of the programmer to adhere-to and optimize-to, but rather as a malleable aspect of the hardware that is an integral part of the overall parallelization of the application by the toolset. For this, we will design a malleable coherence substrate from which we can derive (with the toolset guidance) coherence protocols, especially well-suited for the target application domains. We further innovate by considering not only performance but also power as a first-class constraint in the optimization of the cache coherence.

Our goal is to initially optimize for power-efficiency, but depending on the target application domain, be able to shift the emphasis on performance (e.g., for high-performance computing) or power (e.g., for embedded computing).

Project Coordinator

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Project Partners

COMPAAN DESIGN	NETHERLANDS
UPPSALA UNIVERSITET	SWEDEN
UNIVERSITA DEGLI STUDI DI GENOVA	ITALY
THALES COMMUNICATIONS	FRANCE
SINGULARLOGIC	GREECE
ATHENA	GREECE
POLITECNICO DI TORINO	ITALY
SYNELIXIS	GREECE
ACE ASSOCIATED COMPILER EXPERTS	NETHERLANDS

6.3.8 APPLE-CORE

Apple-CORE will develop compilers, operating systems and execution platforms to support and evaluate a novel architecture paradigm that can exploit many-core chips to the end of silicon. It adopts a systematic model of concurrency implemented as instructions in the processors' ISA (developed in the EU FP6 AETHER project). This has enormous potential but is disruptive, as this paradigm shift requires a new infrastructure of tools.

The benefits are large, however, as compilers need only capture concurrency in a virtual way rather than capturing, mapping and scheduling it. This separates the concerns of programming and concurrency engineering and opens the door for successful parallelising compilers. Mapping and scheduling is performed dynamically by implementations of the concurrency control instructions in the processors ISA. Another advantage of this approach is its binary compatibility. This means backward compatibility over a base ISA and forward compatibility as compiled code is executable on an arbitrary numbers of processors. This compatibility also enables dynamic resource mapping to binary programs from a pool of processors. Particular benefits can be expected for data-parallel and functional programming languages as they expose concurrency in a way that can easily be captured by a compiler.

As well as computational benefit the ISA supports the management of partial failure, which provides support for reliable systems. Finally, this approach exposes information about the work to be executed on each processor and how much can be executed at any given time. This information can provide powerful mechanisms for the management of power by load balancing processors based on clock/ frequency scaling. The objective of developing this infrastructure is to evaluate the model and provide opportunities to exploit the results of this research in a variety of markets, including embedded and commodity processors, and also high-performance applications.

Project Coordinator

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Project Partners

PANEPISTIMIO IOANNINON	GREECE
ACE ASSOCIATED COMPILER EXPERTS	NETHERLANDS
THE UNIVERSITY OF HERTFORDSHIRE	UNITED KINGDOM
GAISLER RESEARCH	SWEDEN
USTAV TEORIE INFORMACE A AUTOMATIZACE	CZECH REPLUBLIC

6.3.9 JEOPARD

The JEOPARD project will develop a platform independent software development interface for complex multicore systems, including SMP. The interface will be based on existing technologies including Java, the Real-Time Specification for Java (JSR 1 and JSR 282) and Safety-Critical Java (JSR 302), which provide a good foundation for the development of complex, safe, realtime systems, but do not yet provide particular support for multicore systems. Even worse, some technologies cannot support more than one processor, making it impossible to develop applications that scale with the number of processors available on current and future advanced multicore systems.

The JEOPARD consortium covers all layers of a multicore embedded system. At the processor level, virtualised SMP architectures and advanced NUMA architectures are addressed. At the OS level, required OS scheduling facilities and low-level OS APIs will be provided for the virtual machine, or low-level native application code. JEOPARD will also analyse the impact of NUMA on OS facilities and how FPGA-based components can integrate with OS-supported components. At the Java virtual machine level, a realtime Java implementation that supports predictable execution of all Java operations will be extended to maintain predictable execution on multiple parallel processors, including real-time memory management, and support for efficient synchronisation mechanisms and compiler support for parallel systems. At the API layer, a powerful interface will be provided that provides control over and efficient use of available processor resources.

Tools for static analysis of parallel applications will also be developed for detection of runtime errors. The project includes close involvement and validation by industry user partners and strong cooperation with standardisation authorities aiming at a POSIX-like standard for multicore systems both at the OS level and Java level.

Project Coordinator

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Project Partners

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UNIVERSITY OF YORK	UNITED KINGDOM
DANMARKS TEKNISKE UNIVERSITET	DENMARK
SYSGO	FRANCE
AICAS	GERMANY
RADIOLABS	ITALY
EADS DEUTSCHLAND GMBH	GERMANY
FZI	GERMANY
GMV SKYSOFT	PORTUGAL
UNIVERSITATEA TEHNICA CLUJ-NAPOCA	ROMANIA

6.3.10 MOSART

The mission of MOSART project is to define and develop an efficient SW/HW design environment encompassing a flexible, modular, multi-core, on-chip platform, and associated exploration methods and tools, to allow the scaling and optimisation of various applications in multimedia and wireless communication.

The project will address two main challenges of prevailing architectures:

- The global interconnect and memory bottleneck due to a single, globally shared memory with high access times and power consumption;

- The difficulties in programming heterogeneous, multi-core platforms, in particular in dynamically managing data structures in distributed memory.

MOSART aims to overcome these through a multi-core architecture with distributed memory organisation, a Network-on-Chip (NoC) communication backbone and configurable processing cores that are scaled, optimised and customised together to achieve diverse energy, performance, cost and size requirements of different classes of applications. MOSART achieves this by:

- Providing platform support for management of abstract data structures including middleware services and a run-time data manager for NoC based communication infrastructure;
- Developing tool support for parallelizing and mapping applications on the multi-core target platform and customizing the processing cores for the application.

The aim is to maintain Europe as a worldwide player in the field of efficient implementation of MPSoC architectures. These ambitious goals are achievable because we bring advanced tools and platforms, i.e. a NoC platform and design space exploration tools from KTH, data management tools from DUT, middleware for NoC services from ART, parallelizing and mapping tools from IMEC, processor configuration tools from VTT. SMEs ART and COW contribute to tools, and two systems companies TCF and ICOM bring applications from future high data rate wireless access.

Project Coordinator

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INTRACOM	GREECE
VTT	FINLAND
INSTITUTE OF COMMUNICATION AND COMPUTER SYSTEMS	GREECE
LT DESIGN SOFTWARE	GERMANY
IMEC	BELGIUM
ARTERIS	FRANCE
KUNGLIGA TEKNISKA HOEGSKOLAN	SWEDEN

6.3.11 VELOX

The adoption of multi- and many-core chips as the architecture-of-choice for mainstream computing will undoubtedly bring about profound changes in the way software is developed. In particular, the use of fine grained locking as the multi-core programmer's coordination methodology is viewed by most experts as a dead-end.

The transactional memory (TM) programming paradigm is a strong contender to become the approach of choice for replacing locks and implementing atomic operations in concurrent programming.

Combining sequences of concurrent operations into atomic transactions promises a great reduction in the complexity of both programming and verification, by making parts of the code appear to be sequential without the need to program fine-grained locks. Transactions remove from the programmer the burden of figuring out the interaction among concurrent operations that happen to conflict when accessing the same locations in memory.

To make TM an effective tool, TM systems will need the right hardware and software support to provide scalability not only in terms of number of cores, but also in terms of code size and complexity. The objective of this project is to understand how to provide such support by developing an integrated TM stack. Such a TM stack would span a system from the underlying hardware to the high end application and would consist of the following components: CPU, operating system, runtime, libraries, compilers, programming languages and application environments.

We anticipate that such a fully integrated TM system will not only improve our understanding of TM designs but also greatly help in the adoption of the TM paradigm by the European software industry, making it a tool-of-choice for concurrent programming on multi- and many-core platforms.

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ECOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE	FRANCE
TECHNISCHE UNIVERSITAET DRESDEN	GERMANY
ADVANCED MICRO DEVICES	GERMANY
RED HAT	IRELAND
TEL-AVIV UNIVERSITY	ISRAEL
UNIVERSITE DE NEUCHATEL	SWITZERLAND

7 EU actors in EU funded Computing Systems research

7.1 Overview

There are several distinguishing characteristics between actors that carry out Computing Systems research in India and the EU. One factor is the number of actors involved in Computing Systems research. In India, the total number is less than 20 organisations, while

in the EU more than 160 organisations are involved in EU funded Computing Systems projects. Another factor is the types of organisations that carry out the research projects. In India, there is no direct participation in government funded Computing Systems research by industrial actors. All of the Indian projects are awarded to research institutes, government supported agencies or universities. In the EU, there is industrial actor participation in nearly every funded Computing Systems project.

If the projects funded by the ARTEMIS Joint Undertaking focused on embedded systems in the EU are considered, the number of EU organisations involved in government funded projects addressing Computer Systems technologies jumps to over 700. However, it's important to note that ARTEMIS Joint Undertaking projects are majority funded directly by EU member states with the European Commission providing only a small percentage of funding (16.7%), and not all EU member states provide funding or in some cases the funding levels are at relatively low levels. A more analogous relationship exists between participation in Indian and EU government funded projects in Computing Systems when the focus in the EU is on projects funded directly by the European Commission under the FP7 Programme.

While the European Commission's FP7 Programme provides financial support to Indian organisations to participate in EU funded projects, there are not any Computing Systems research and development projects under FP7 that benefit from the participation of an organisation from India. The EU-INCOOP partners believe an important opportunity for collaboration between the EU and India is increased participation in Indian organisations participate more in EU funded research and development projects.

7.2 EU actor participation

The challenge for Indian organisations interested in participating in EU funded research projects is becoming part of an EU-centred consortium that prepares a successful project proposal. While the EC evaluation procedures are designed to ensure a level playing field amongst those seeking funding at each Call, an analysis of EU funded projects and the actors involved show there are several EU actors who are especially active and successful in participating in EU research in Computing Systems funded directly by the European Commission.

There are a total of 168 actors[3] currently involved in EC Computing Systems projects funded directly by the European Commission. The distribution of the frequency of project participation by actor is shown in Figure 7. The majority (95 out of 168) of actors participate, or have participated, in only one EU funded project. A sizeable number of actors (44) participate in two projects, while far fewer actors participate in three or more projects.

[3] This number will be slightly lower than EC figures as it combines legal entities from the same organisation that are located in different countries. The EC system typically counts each legal entity as an individual project participant.

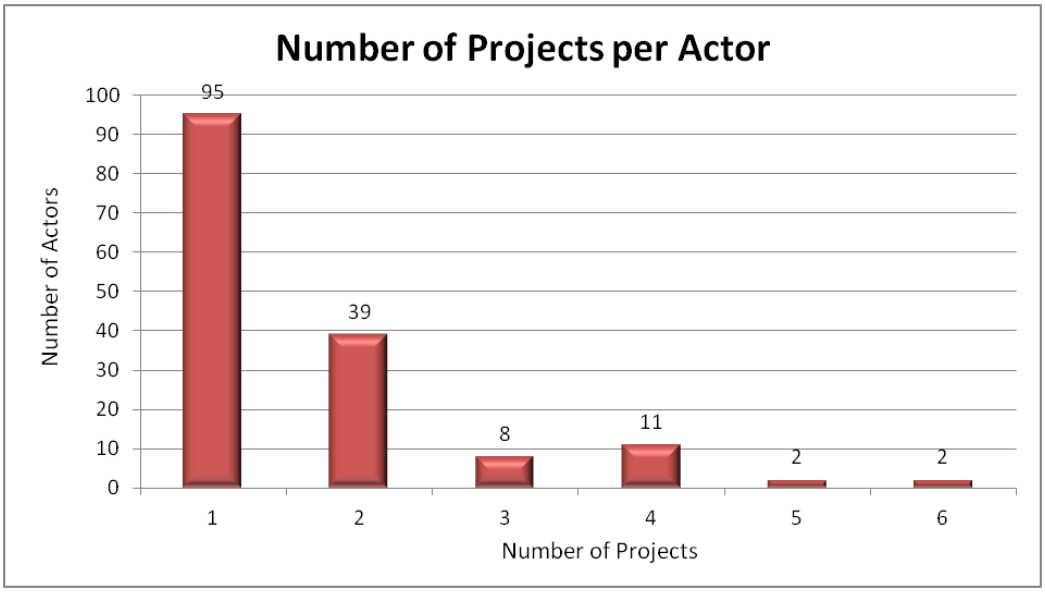

Figure 7: Frequency of EU Computing Systems projects by actor

7.3 Key EU Computing Systems actors

While past success in obtaining EU funding for projects is generally not an indicator of future success due to strict transparency of European Commission proposal evaluation procedures, there are actors that are more broadly involved in EU funded Computing Systems research projects than others. This will usually be due to a combination of factors ranging from technical expertise focused in Computing Systems technologies, to experience in preparing well structured proposals, to having well-established academic and industrial collaborations to be able to assemble strong consortia, and several other factors.

When an Indian organisation interested in participating in EU funded projects has a choice of EU actors to work with, one element that might be worth considering when deciding who best to collaborate with is the degree to which an EU actor is already involved in EU funded projects. Figure 8 identifies the actors in Computing Systems projects that have three or more projects that have been funded directly by the European Commission under the FP7 Programme.

A further consideration that results from the numbers in Figure 8 is that an Indian organisation doesn't have to manage a very large number of EU contacts to be strongly connected into EU funded research. There are a total of 38 projects funded so selecting just a handful of EU actors to work with who are involved in multiple projects would allow Indian actors to link into more than half of the EU funded projects in Computing Systems funded directly by the European Commission.

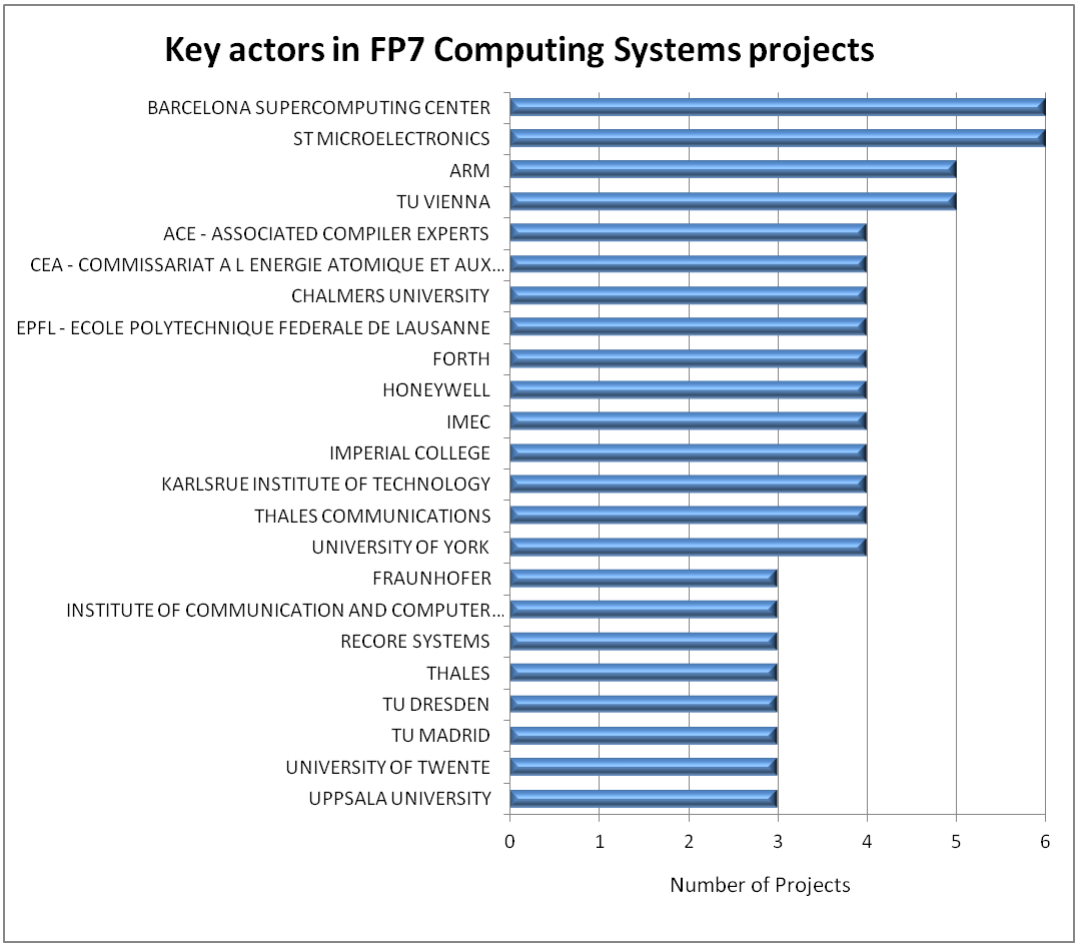

Figure 8: EU actors involved in 3 or more Computing Systems projects

Specific contact details are not provided for the actors shown in Figure 8 as often different projects are handled by different departments or in some cases different locations of the actor. However, Indian organisations seeking to get more involved in EU funded projects can find contact details by using the EC search facilities found at: http://cordis.europa.eu/fp7/ict/projects/home_en.html to obtain project and partner information, and more detailed contact information may be found at nearly all of the EU project websites.

7.4 Geographic locations of key Computing Systems actors

Figure 9 shows the geographic locations of the key actors in Computing Systems projects that have three or more projects funded directly by the European Commission.

Figure 9: Geographic locations of EU actors involved in 3 or more Computing Systems projects

There is a slight concentration of key actors in France, Germany, United Kingdom and the Netherlands, with each having three or more key actors in Computing Systems research directly funded by the European Commission. The main consideration that results from the distribution shown in Figure 9 is that Indian organisations seeking to collaborate with EU contacts having the most experience in EU funded projects in Computing Systems will find nearly all of these organisations in the older member states of the EU (i.e. sometimes referred to as Western Europe). Organisations from these countries have benefited from participation in EU funded research for more years than partners located in the new member states of the EU. However, it's also worth noting there are competent organisations for project partnering in every EU member state.

7.5 Key EU actors in ARTEMIS projects

The ARTEMIS Joint Technology Initiative is implemented as a Joint Undertaking (JU) formed as a public-private partnership between the following:

- European Commission
- Participating Member States of the EU – not all provide funding for ARTEMIS
- ARTEMIS Industry Association – operating as a non-profit member based association

The ARTEMIS JU is a legal entity based in Brussels, which was formally established in February 2008 and became autonomous in October 2009, and is managed by an Executive Director. ARTEMIS aims to tackle the research and structural challenges faced by European industry by defining and implementing a coherent Research Agenda for Embedded Computing Systems.

The ARTEMIS JU supports research and development activities through open and competitive calls for proposals published on a yearly basis aiming to attract the best European research ideas and capacities in the field of Embedded Computing Systems. Proposals submitted to the ARTEMIS JU undergo a technical evaluation and selection process carried out with the assistance of independent experts similar to project proposals submitted to the European Commission for direct funding, however the national funding by EU Member States and the varying national requirements each Member State establishes for ARTEMIS JU participation results in a different mix of organisation types (research vs. industry) that participate as compared to projects directly funded by the European Commission.

Another effect that is seen with ARTEMIS JU projects is a higher frequency of organisations being involved in multiple projects as is shown in Figure 10. The maximum number of participation in projects seen for Computing Systems projects funded directly by the European Commission was 6 projects, achieved by only two EU actors. However, within the ARTEMIS JU projects there are 14 actors involved in 8 or more of the 52 ARTEMIS JU projects, and one actor from Spain is involved in 23 or nearly 44% of all ARTEMIS JU projects.

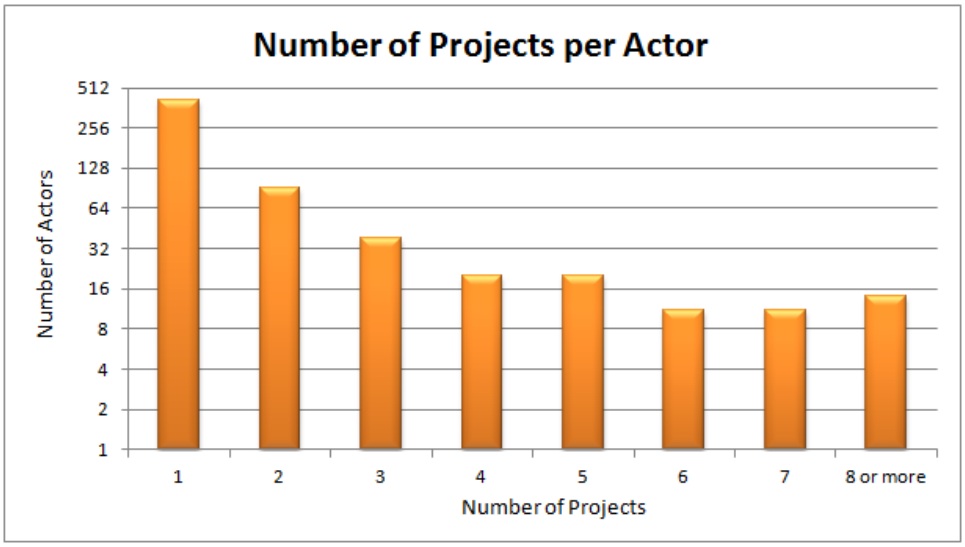

Figure 10: Frequency of ARTEMIS Embedded Systems projects by actor

The total number of actors participating in ARTEMIS JU projects is nearly four times larger than those participating in projects directly funded by the European Commission (157 actors vs. 625 actors). This is due to the ARTEMIS JU embracing several very large projects that involve 60 or more actors, which is a project funding strategy the European Commission does not engage in for directly funded Computing Systems projects.

For Indian organisations with specific interests in collaborating in Embedded Systems technologies there are a wide choice of EU actors as potential collaborators as there are

many organisations involved in multiple ARTEMIS JU projects. Figure 11 identifies the actors in ARTEMIS JU funded projects that have six or more projects that have been funded.

As is the case with Computing Systems projects directly funded by the European Commission, from the numbers in Figure 11, it is clear that an Indian organisation interested Embedded Systems collaborations does not have to manage a large number of EU contacts to be strongly connected into ARTEMIS JU funded projects. Selecting just two or three EU actors for collaboration involved in multiple projects would allow Indian actors to link into more than half of the Embedded Systems projects funded by the ARTEMIS JU.

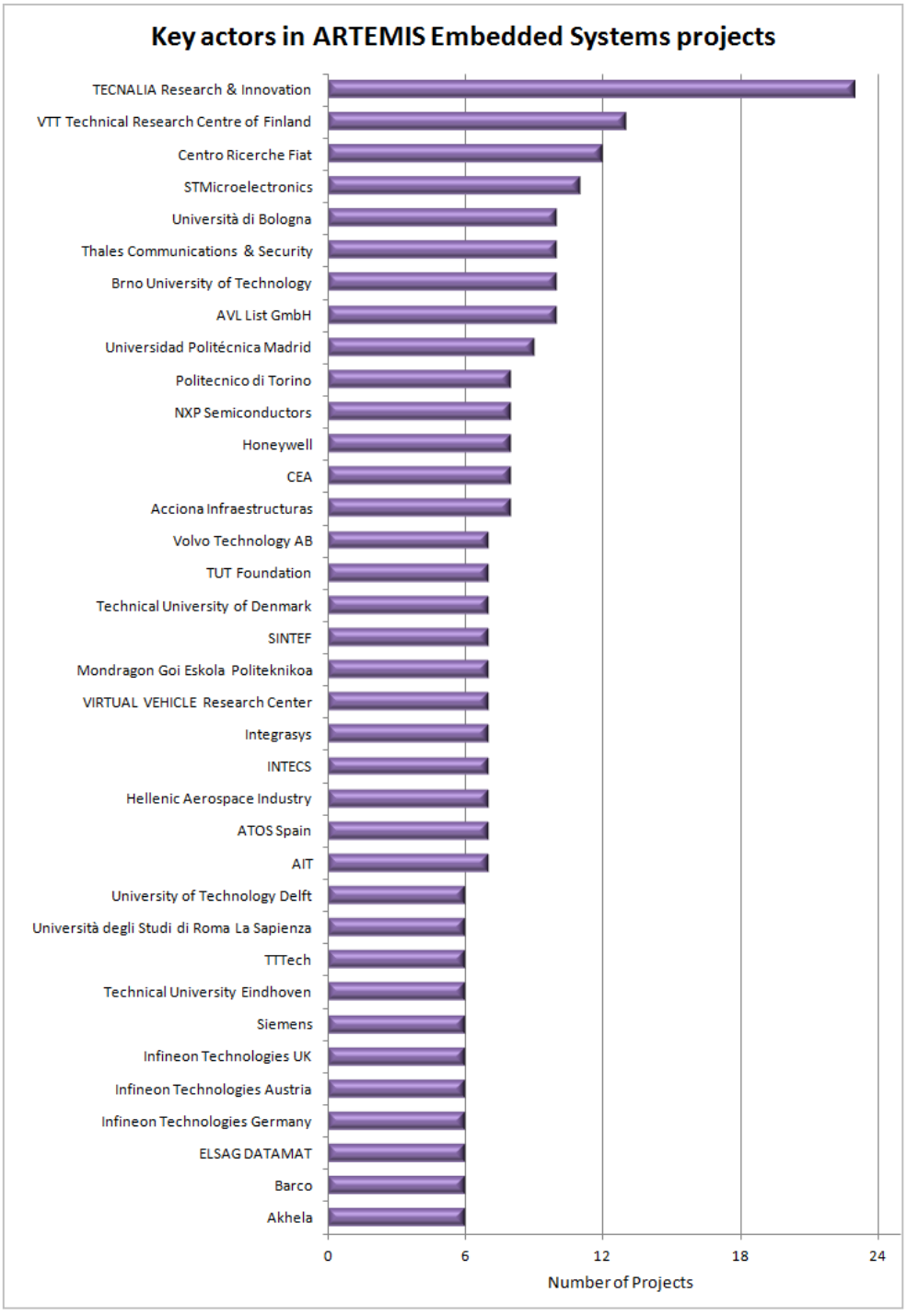

Figure 11: EU actors involved in 6 or more ARTEMIS Embedded Systems projects

Specific contact details are not provided for the actors shown in Figure 11 as often different projects are handled by different departments or in some cases different locations of the actor. However, Indian organisations seeking to get more involved in ARTEMIS JU funded projects can find contact details by using the ARTEMIS JU search facilities found at: http://www.artemis-ia.eu/call_projects to obtain project and partner information, and more detailed contact information may be found at nearly all of the ARTEMIS JU project websites.

7.6 Geographic locations of key ARTEMIS JU actors

Figure 12 shows the geographic locations of the key actors in Embedded Systems projects that have six or more projects funded by the ARTEMIS JU.

Figure 12: Geographic locations of EU actors involved in 6 or more ARTEMIS JU projects

There is a concentration of key actors in Italy, Spain and Austria with each country having five or more actors involved in six or more Embedded Systems projects funded by the ARTEMIS JU.

ARTEMIS JU projects are not well-suited for direct participation from Indian actors if funding is required as the majority of funding for ARTEMIS JU projects is provided by EU members states and is only available to organisations in the respective EU countries, however, collaboration with Indian actors, and in particular opening industrial opportunities in India in

collaboration with Indian actors, for technologies developed under ARTEMIS JU funding would likely be of interest to many EU actors participating in ARTEMIS JU projects.

8 EU / India research topics analysis

8.1 Methodology

The analysis comparing the Computing Systems research topics addressed by EU and India funded projects utilised the same methodology for identifying EU funded Computing Systems projects that are related to projects in India described in Section 6.2. The first step of the analysis involved reviewing India funded projects to determine the extent to which the projects addressed the following eight technology areas:

- Multicore
- Virtualisation
- Parallelisation
- Platform and Hardware
- Performance Analysis
- Predictability
- Reconfigurability
- Composability

These technology areas[4] were derived from a review of all 38 EU Computing Systems projects to identify the main research areas; therefore, all of these categories are addressed to some degree in the EU research projects. This can be seen in Figure 13, where the number of EU funded projects that address each topic is shown and where every topic is addressed by one or more projects. (Note that projects often address more than one topic so the cumulative frequency of all topics will be greater than the total number of EU funded projects.)

[4] Further explanation of the technology areas are provided in Section 6.2.

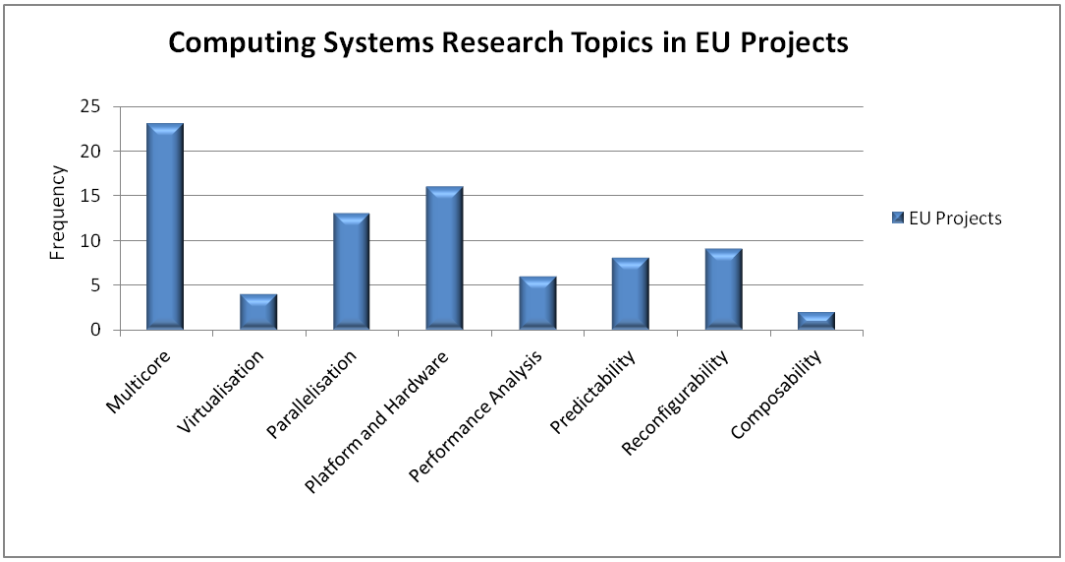

Figure 13: Prevalence of Computing Systems research topics in EU funded projects

8.2 Comparison of EU and Indian research topics

The review that was carried out of the 40 India funded Computing Systems projects determined the extent to which they were addressing topics similar to those of the EU projects funded by the European Commission. Figure 14 shows the prevalence of these eight topics being addressed in India funded projects.

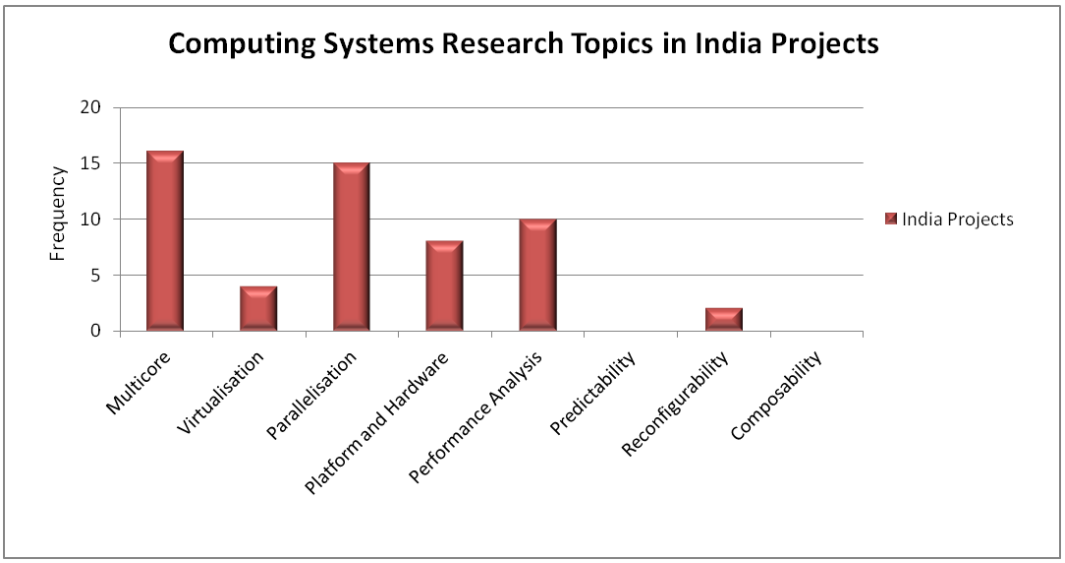

Figure 14: Prevalence of EU Computing Systems research topics in India funded projects

The analysis showed there were several topics that were of common interest. It also identified that there were two areas where EU research was addressing topics that were not generally being addressed in India. These were technologies and tools for ensuring the predictability of systems (i.e. for hard real-time applications), and technologies for developing composable systems.

Figure 15 provides a comparison of the prevalence of the eight Computing Systems topics in both EU and India funded projects.

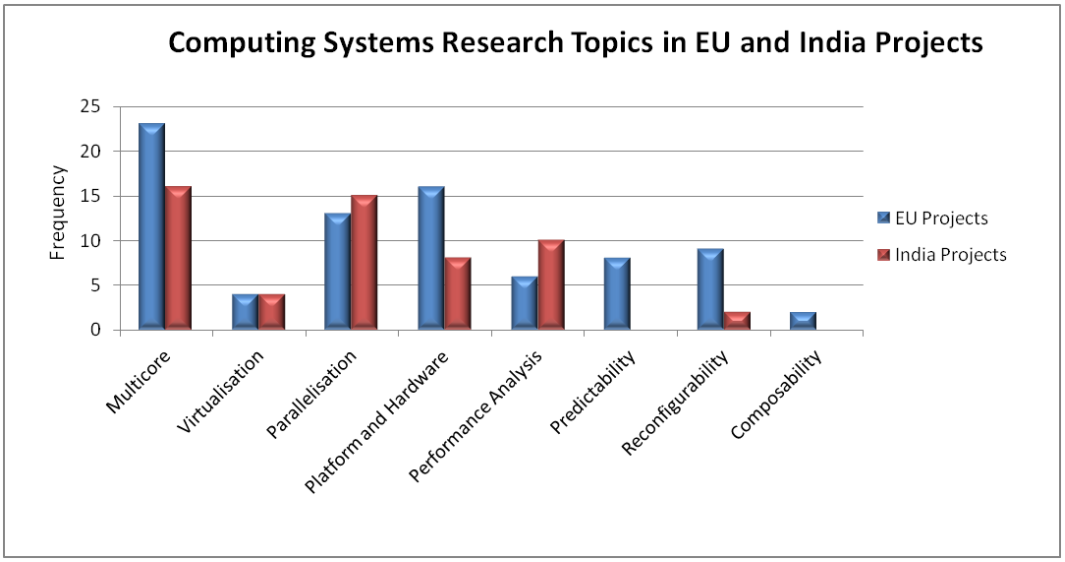

Figure 15: Comparison of Computing Systems research topics in India and EU funded projects

As the number of research projects evaluated in India and the EU are nearly equal, it's possible to make the following observations:

- The EU has a greater number of projects addressing research into multicore technologies than India. This is likely related to the emphasis placed in India on applying advanced technologies like multicore, while the EU is investing in the design and development of advanced multicore platforms.
- Both the EU and India have similar levels of interest in the use of virtualisation technologies.
- Both the EU and India have similar levels of interest in technologies for improving parallelisation of systems. India has a few more projects, though some of these are more about applying advanced parallelisation techniques for specific application domains rather than researching new parallelisation techniques.
- The EU has a greater number of projects addressing the platform and lower level system technologies than India. The motivation behind this is likely to be the same as the EU's greater emphasis on multicore research.
- India has a larger number of projects that are focused on performance analysis and optimisation, though as in the case with parallelisation some of these are more about applying performance analysis techniques to address specific application domains needs rather than developing new techniques.
- Reconfigurability plays a larger role in EU funded projects than in India research. The area for India projects where research into reconfigurability is most prevalent are related to Ubiquitous Computing.

These observations made early in the work programme of the EU-INCOOP project will be further investigated and areas for future collaboration will be identified as the EU-INCOOP project progresses.

As a final step in the comparison of India and EU funded project topics, a review was carried out of Indian projects to identify topics addressed in India that were not being addressed by

EU funded Computing Systems research. The topics identified from the 40 Indian projects were the following:

- Data management technologies – research topics in this area appear frequently driven by the needs of specific applications domains (e.g. medical analysis and health management services)
- Analytical engines – these sometimes overlap into the high performance and multicore categories, however, there are several specific projects in India where computational engines are being developed to address several different types applications.
- Sensors and sensor networks – a few projects are developing new techniques for handling sensor networks, aggregating and passing data in real-time.
- Merging Grid and Ubiquitous Computing technologies – this is an area that has multiple subprojects in India where technologies in the subprojects related to Grid computing and reconfigurable systems are similar to those in EU Computing Systems.
- Neural networks – India is investing in further development of neural networks and bio-inspired computing systems.
- Technologies for handling language – Indian has several projects developing system level technologies to address the multiple natural languages spoken in the country.

The EU-INCOOP project partners list the above areas recognising that the scope of the evaluation was focused in the EU on funded projects from the FP7 Computing Systems objective. If the scope of analysis was slightly expanded to include other ICT objectives of the European Commission related to the Internet of Things, Language Technologies, Intelligent Information Management, and others, it's clear that nearly all of the topics addressed by India funded research projects would have some counterpart for research and development within EU funded projects under FP7 for ICT. The opportunity for EU / India research collaboration clearly extends beyond the EC Computing Systems objective.

9 Considerations for coordinated EU / Indian project funding

The ultimate goal of the EU-INCOOP project is to identify a shared set of research priorities and roadmap between the EU and the India through the involvement of both EU and Indian actors. The roadmap will provide the foundation for what might eventually be a coordinated call[5] between the EU and India providing funding for both EU and Indian organisations to work together. The objective of a coordinated call would be to create closer collaboration between Computing Systems research activities in each region.

Some recommendations have been identified in the course of cataloguing the actors and projects in Indian and the EU that may need to be considered when constructing a

[5] The term Coordinated Call is used as it's not yet clear if the most appropriate approach for greater collaboration is a single Call, or two parallel Calls timed in each region, or some other mechanism.

coordinated call between the regions. While the EU-INCOOP project is still in the early phases, a first set of recommendations are as follows:

- Focusing on a single ministry for collaboration in India will likely be more fruitful for a coordinated call. The decentralised nature of Indian research funding creates an added level of complexity in coordinating a Roadmap, schedules, and funding amounts and is highly political. While involving additional Indian ministries might mean a more substantial initiative in terms of total research funding from India, it's probably a better strategy to move quickly with one ministry than to attempt to work the political challenges of coordinating the collaboration of two ministries.
- Each of the Indian funding sources includes procedures for establishing research topics to be funded through advisory committees or councils of experts and stakeholders. It is unlikely that Indian funding sources will move forward with a coordinated call without some level of support from their advisory committee. Some extended effort will likely be needed to brief and gain the support of these advisory groupings.
- India research in Computing Systems is more often focused on technology infrastructure or deployment of technologies for specific application domains. These aspects will be important elements to consider and potentially include within any eventual coordinated call.
- Some Indian funding sources have experience in creating calls for research projects that are jointly funded by government and industry sources. The calls are coordinated by government organisations following typical government evaluation and selection procedures, but commercial organisations also contribute to the available funding. Such an approach in India for a coordinated call might prove worthwhile to explore for achieving parity in funding levels from India and the EU for new Computing Systems projects.

Further considerations will likely be identified by the EU-INCOOP project partners as work progresses and further interactions are orchestrated amongst the key actors from each region.