SEVENTH FRAMEWORK PROGRAMME

System-on-chip Fault-Tolerance: **the DeSyRe approach**

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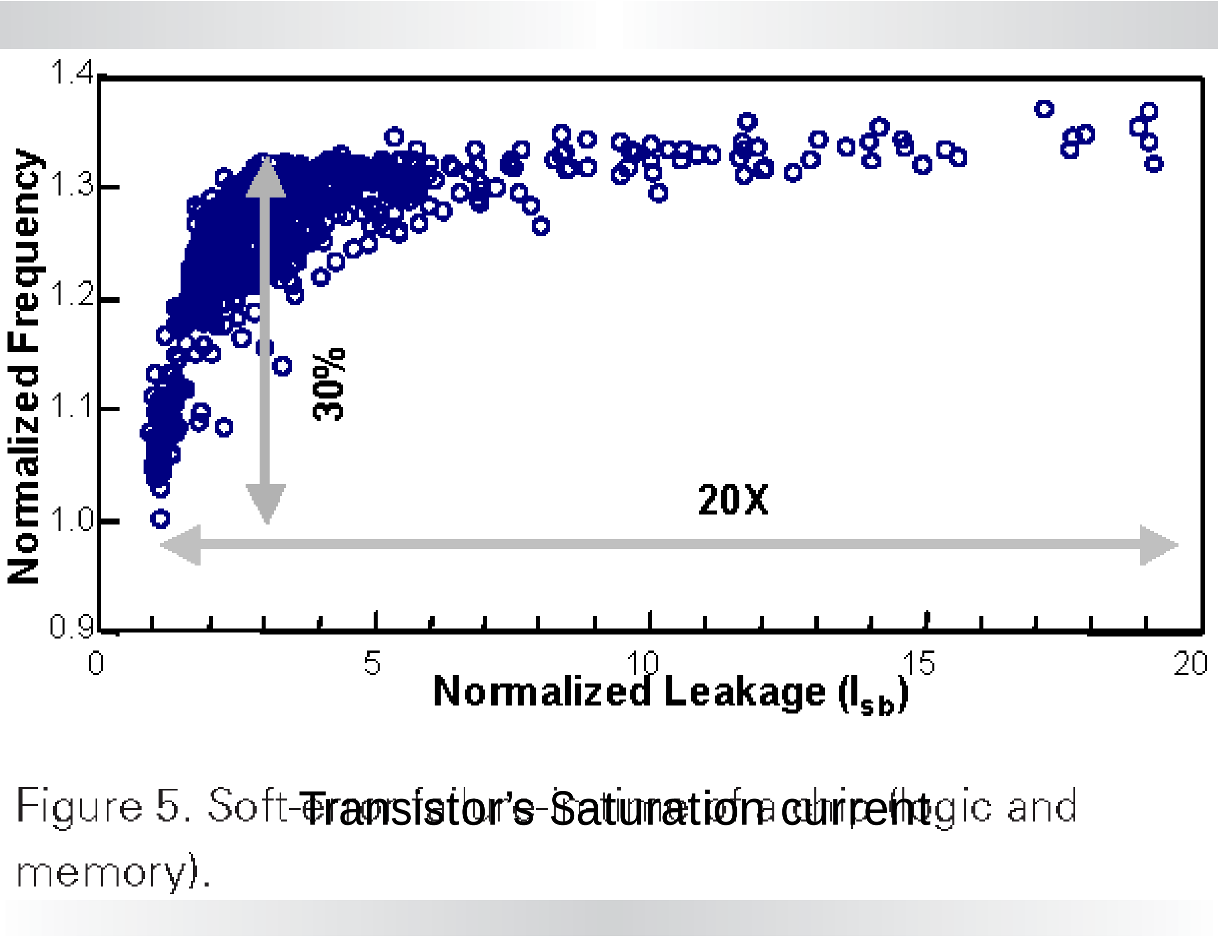
DeSyRe
on-Demand System Reliability

Technology trends

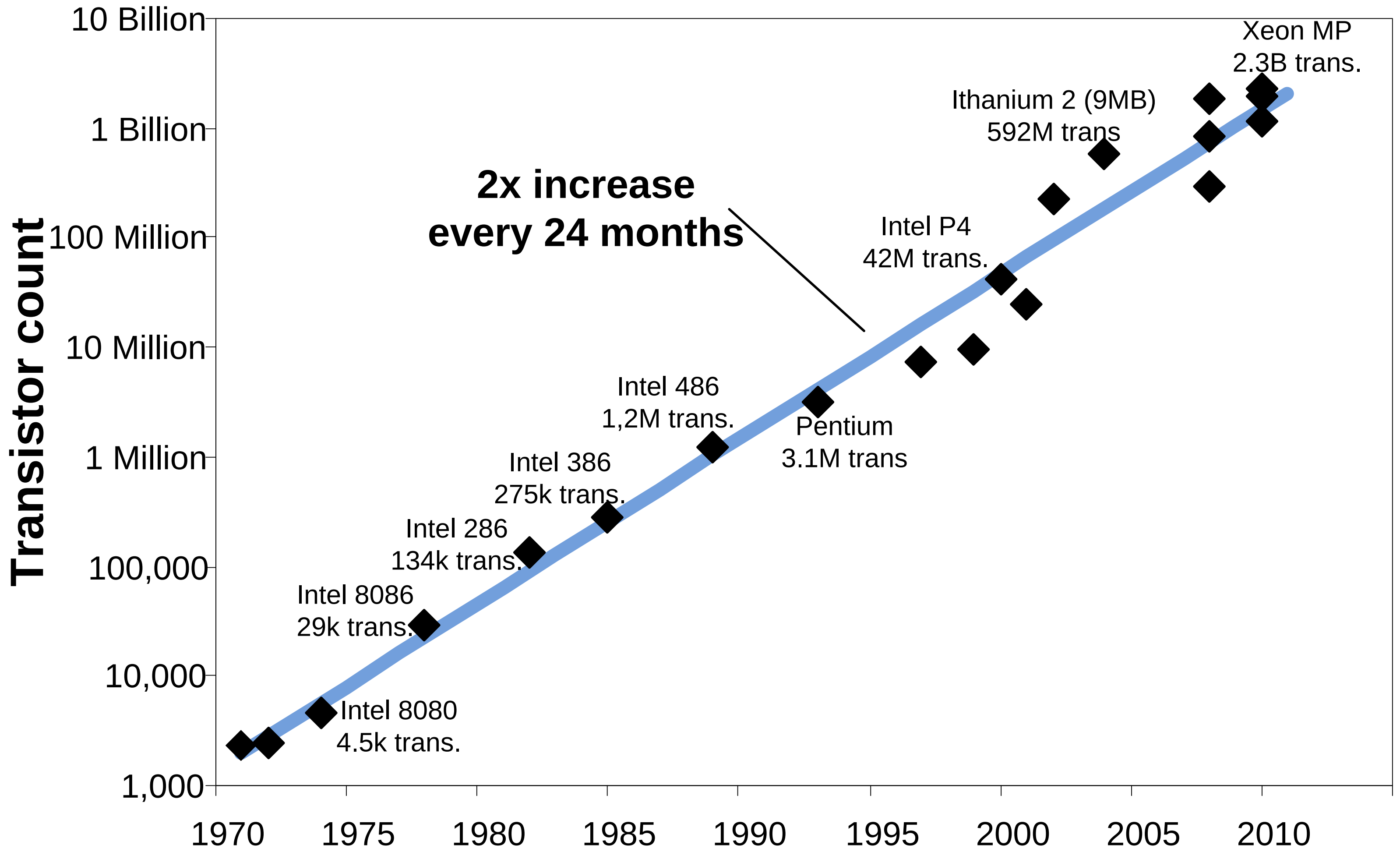
As Technology Scales chips are becoming less reliable

- Harder to keep defect density constant
  - **Manufacturing cost increases**
- Variations become more severe
- Transistor aging is accelerated
- Soft-error rate grows exponentially
  - **mostly logic state bits**



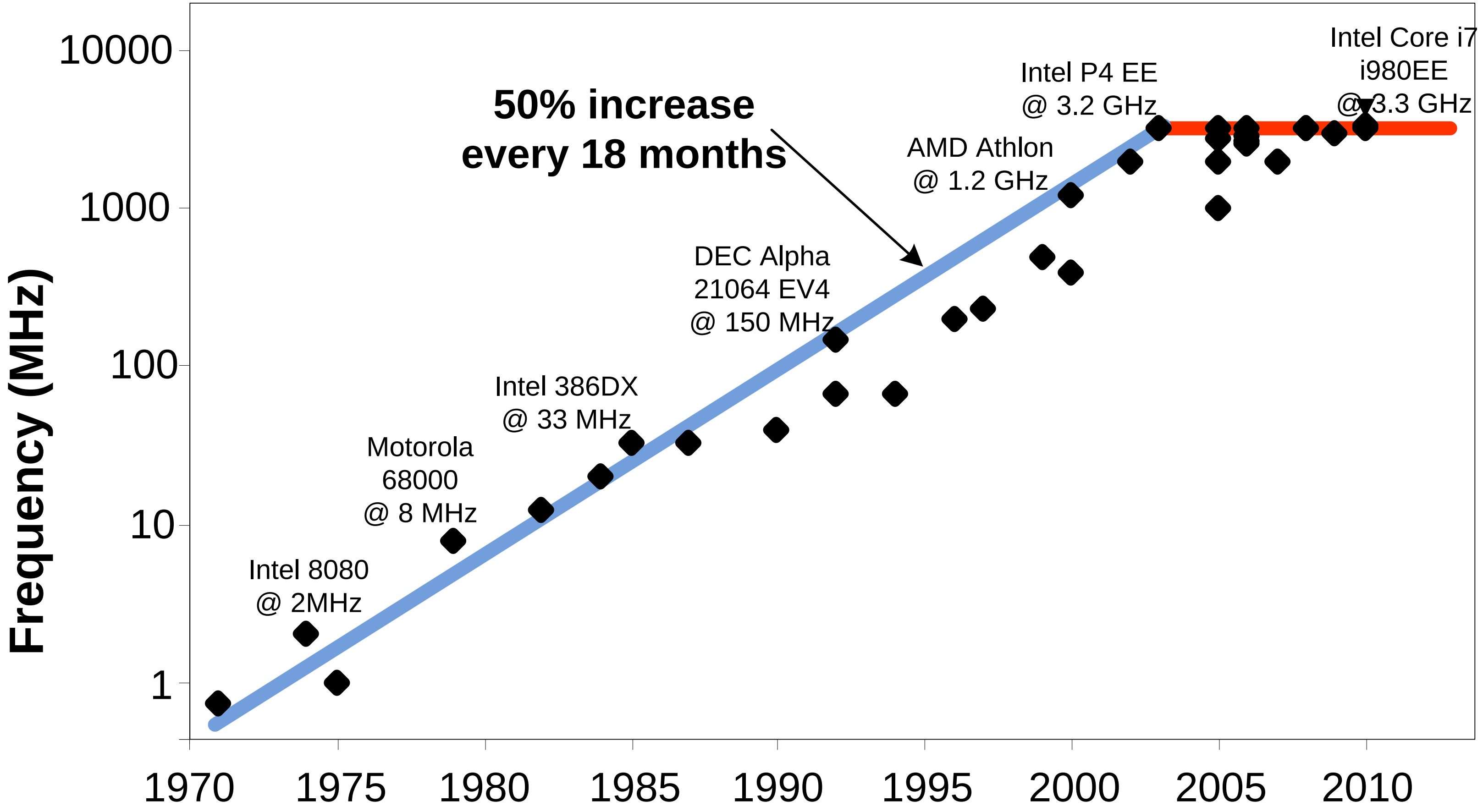
Transistor's Saturation current

Transistor count



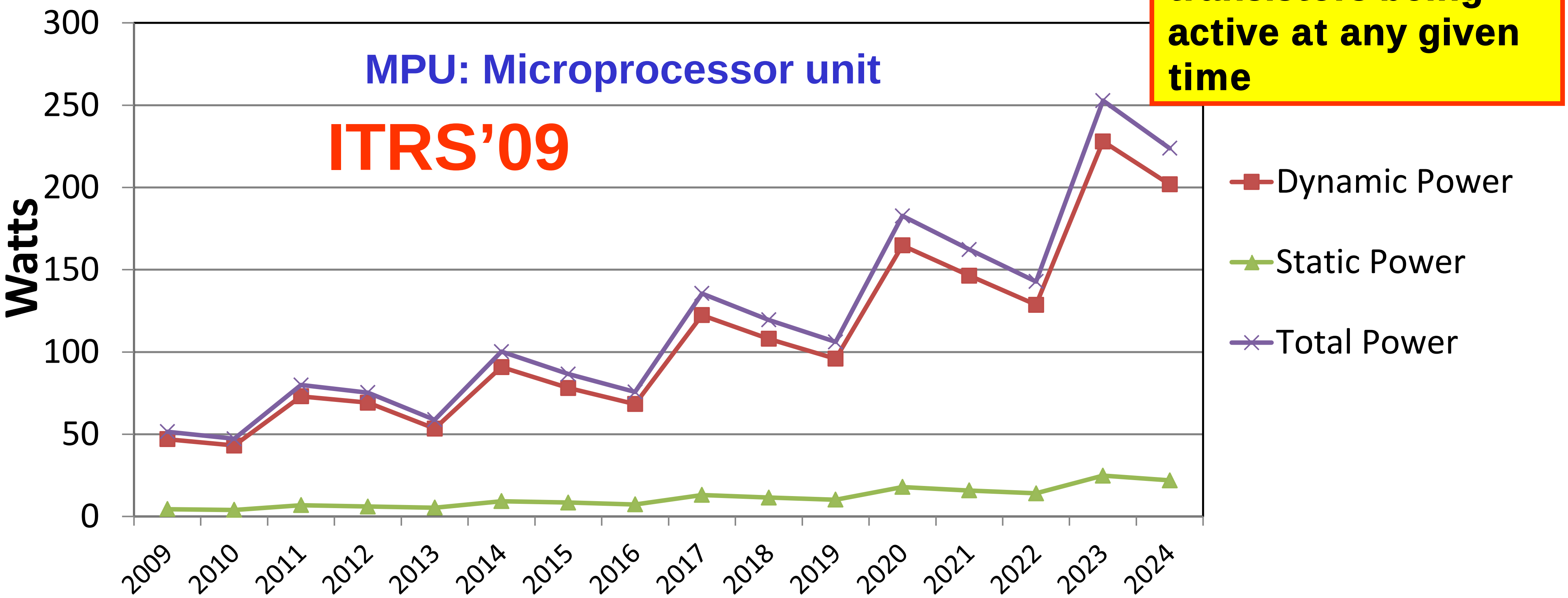
- On-chip resources keep increasing

Performance trends



- New technology nodes do not deliver significant Performance improvements

Power trends



MPU: Microprocessor unit

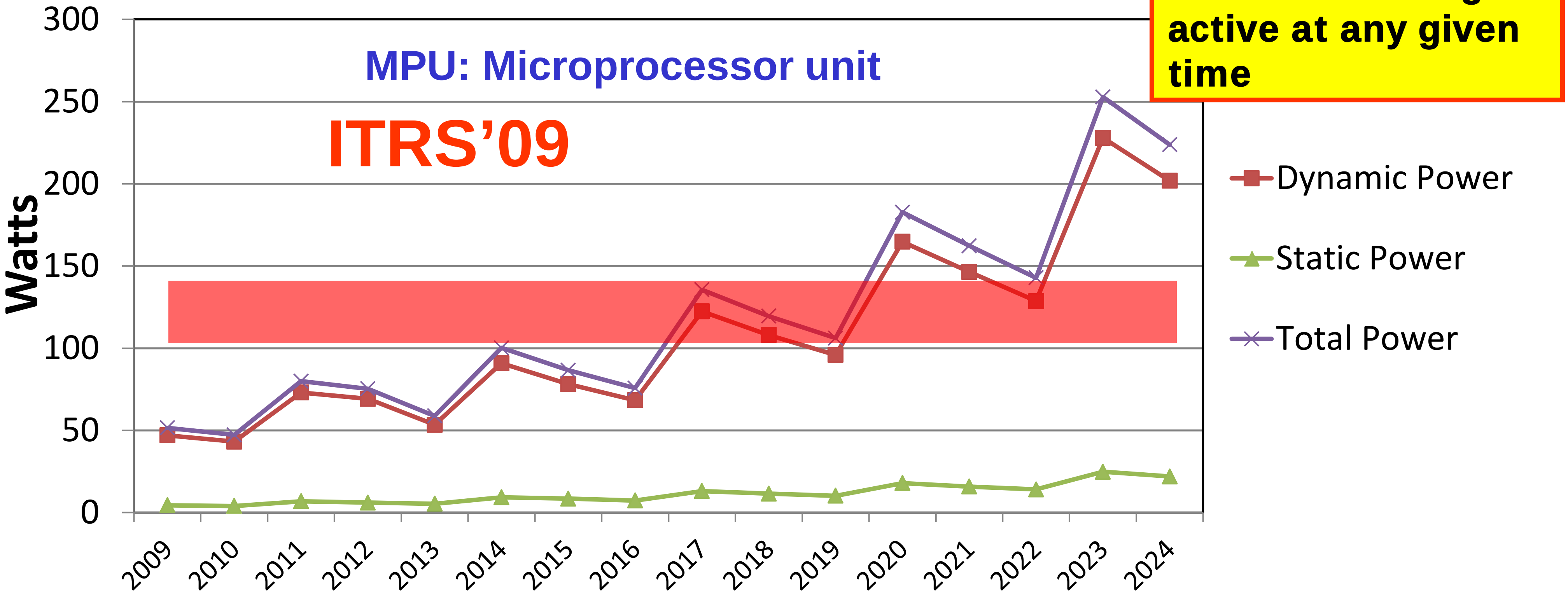
ITRS’09

For 40% of the transistors being active at any given time

- Power consumption is a major limiting factor

Power density limits gate density

For 40 % of the transistors being active at any given time



- **By 2018 chips will exceed the max allowed power consumption:**
  - Then significant parts of a chip will need to be inactive to stay within the available power budget

The Cost of Fault Tolerance

Fault Tolerance requires Redundancy

- **in time:**
  - **Performance** overhead
- **in space:**
  - **Power** and **Area** overhead
- **Both in time and space:**
  - **Energy** overhead

DeSyRe:
on-Demand System Reliability

- Generic design framework for future reliable SoCs
- **Main Goal:**
  - to reduce the costs for fault tolerance
- **How?**
  - Flexibility/reconfigurability
  - System-level support for dynamic adaptation
- **Applications:** DeSyRe will be applied to two Medical SoCs

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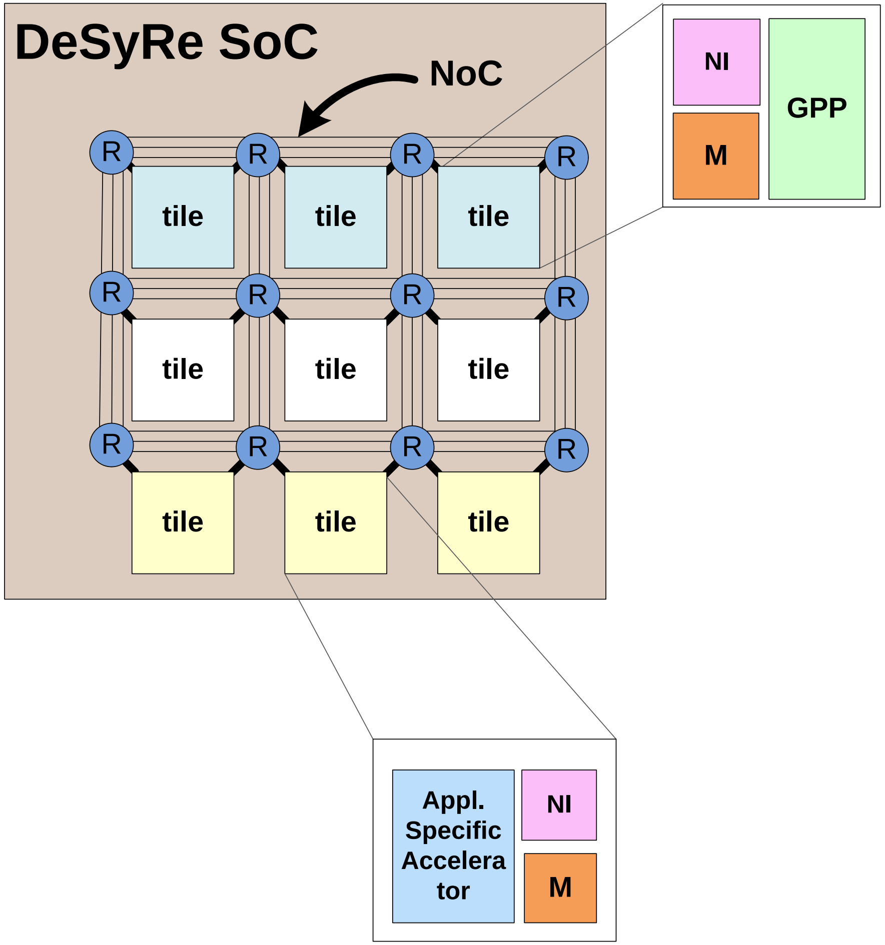


DeSyRe objectives

Develop a generic design framework for heterogeneous embedded SoCs, to:

1. **Provide reliability at a reduced performance, energy and power cost.**
   - ❑ tolerate permanent, intermittent and transient faults

2. **Reliable by Design** (for fabless chip developers)
   - ❑ Guarantee reliability of chips by design
   - ❑ Technology independent

3. **Build on-demand adaptive systems.** Systems built on flexible/reconfigurable hardware complimented by system-level techniques. Adaptive to
   - ❑ **Various types of faults**
   - ❑ **System constraints** (power, energy, resources)
   - ❑ **Application requirements** (performance constraints, reliability requirements/safety/availability)

4. **Increased Defect tolerance** (design, manufacturing defects, defects due to aging).
   - ❑ Increased manufacturing yield
   - ❑ Longer SoC lifetime
   - ❑ Lower manufacturing cost
   - ❑ Shorter time-to-market

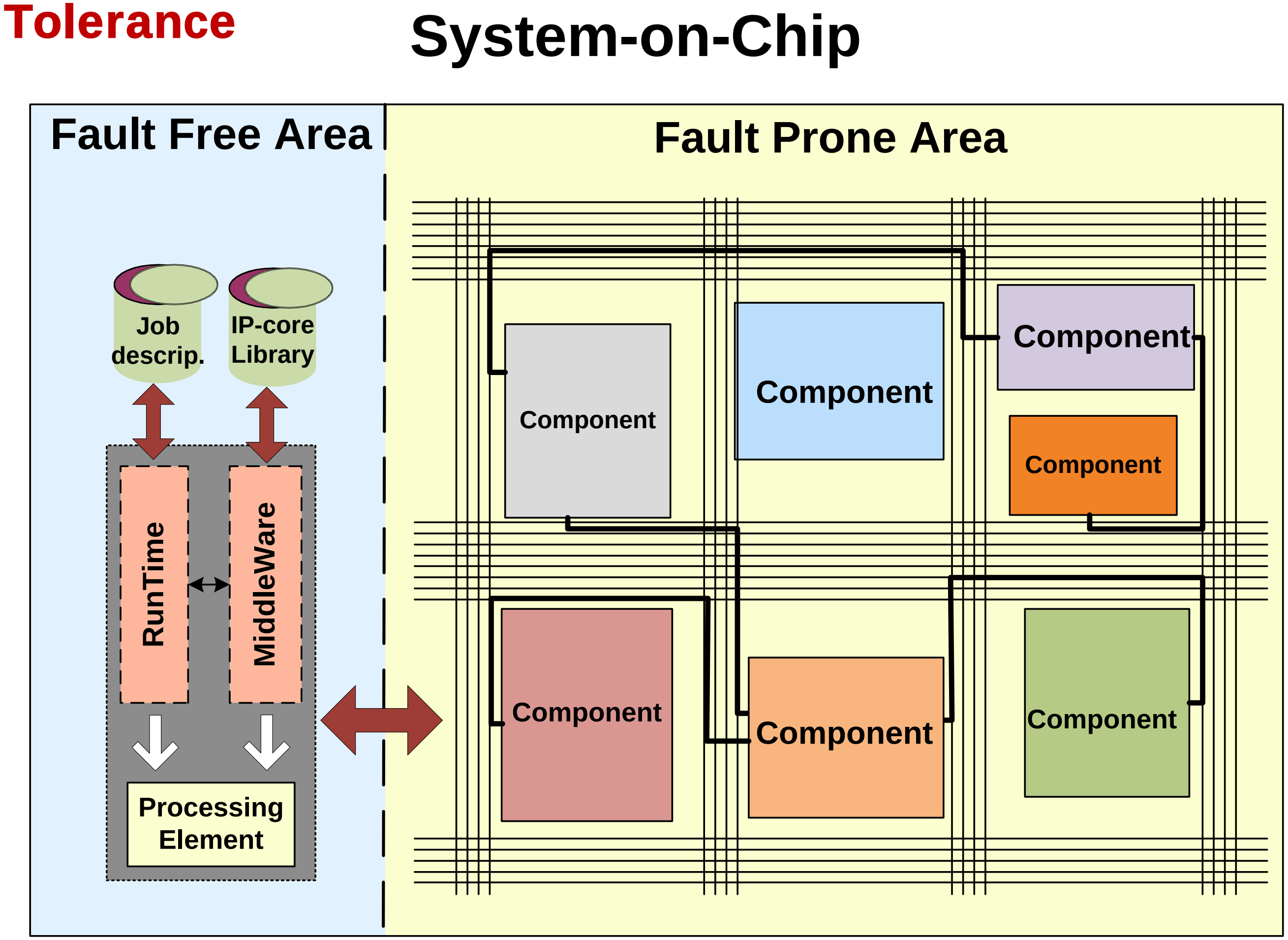
The DeSyRe design framework

- Only a small fraction of the chip will be designed to be **Fault Free.**
  - To **Reduce Cost for Fault Tolerance**

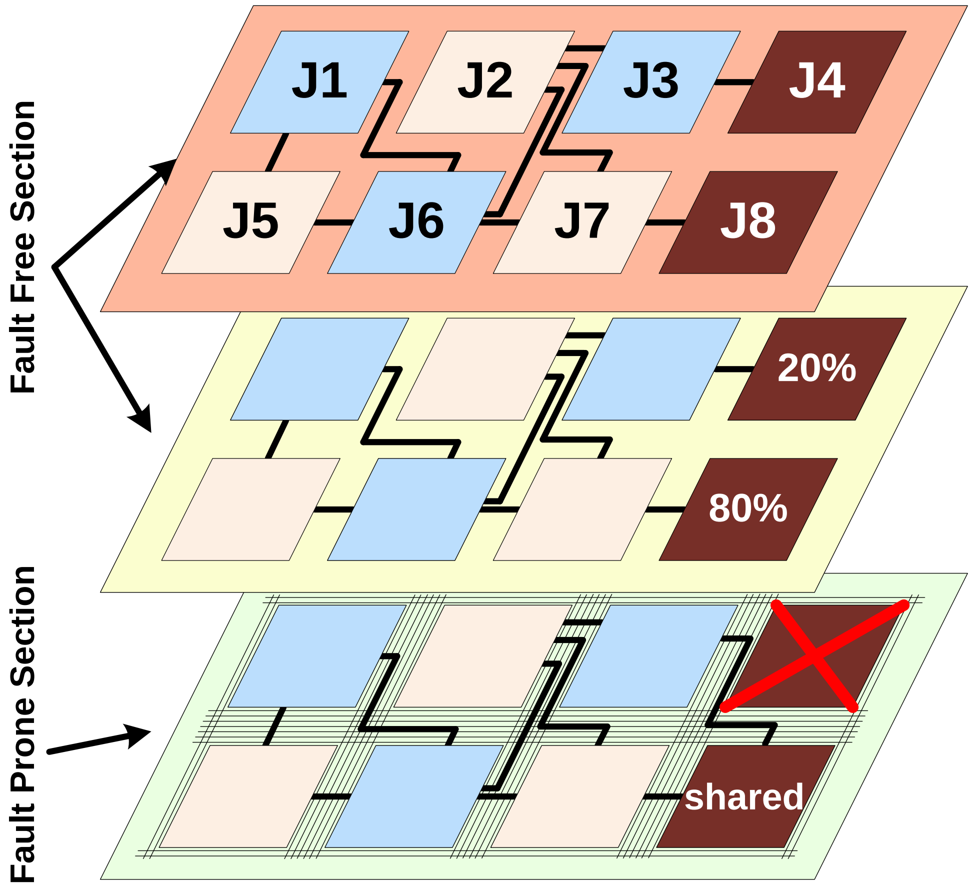
- Fault Free part will manage the remaining unreliable resources.

- The remaining **Fault Prone resources** will provide **flexibility reconfiguration**

- System reliability managed at **runtime** based on the:
  - Application requirements
  - System constraints
  - Fault types and density



DeSyRe framework layers



Runtime System
Software-layer

MiddleWare
Software-layer

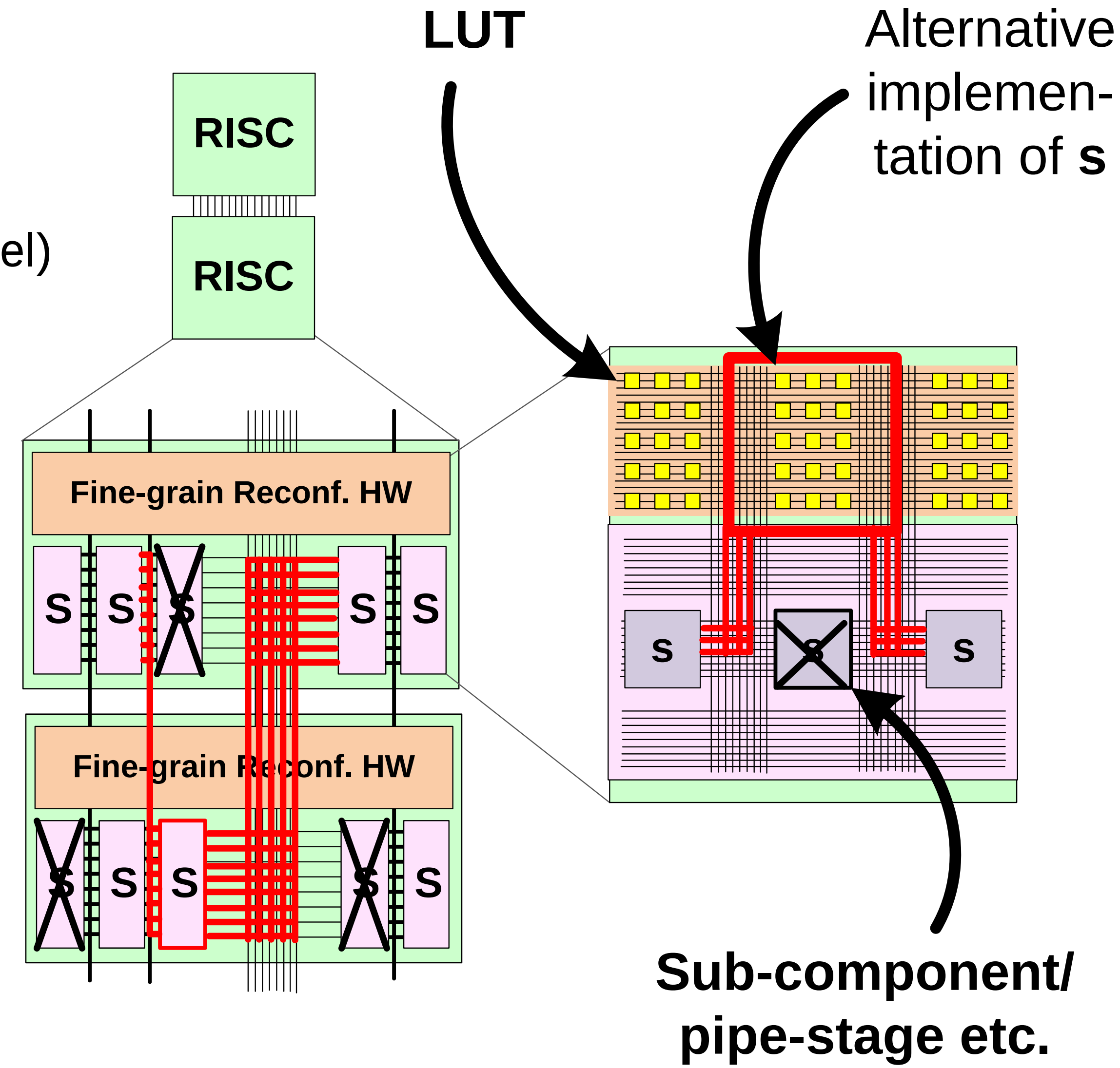
Components:

1. Component Architecture
2. Realization (HW Substrate)

DeSyRe Reconfigurable Substrate

- **Two levels of Reconfiguration:**
  1. Coarse-grain (Component-level)
  2. Fine-grain (FPGA-like)

- **Example: RISC processor**
  - partitioned in pipeline stages
  - Reconfigurable wires for interconnection
  - Fine-grain reconfigurable blocks


RISC
RISC
Fine-grain Reconf. HW
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S
Fine-grain Reconf. HW
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LUT
Alternative implemen-tation of **s**
s
s
s
Sub-component/ pipe-stage etc.

SEVENTH FRAMEWORK PROGRAMME

Fault Types: causes / DeSyRe solutions

- **Permanent faults:**
  - Cause:
    - Manufacturing process or Aging
  - Detection (diagnosis):
    - Online and offline testing managed by the fault-free part (or even locally)
  - Correction:
    - System Reconfiguration: isolate, replace/task migration /reconfigure

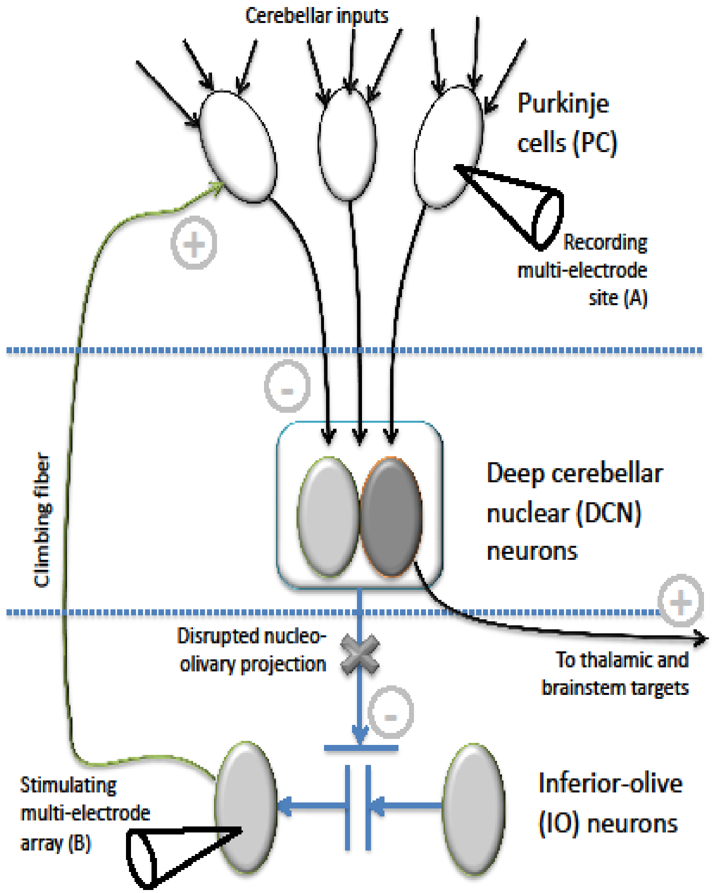
- **Transient Faults:**
  - Cause:
    - Radiation, ɑ-particles, etc
  - Detection:
    - Local checkers per tile
    - Checkpoints set by the fault-free part
  - Correction:
    - Checkpointing (HW assisted): recover and re-execute
      - based on the application needs
    - ECCs

- **Intermittent Faults:**
  - Cause: variations (process, temperature, etc.)
  - Detection: same as transient (+ extra step to distinguish form transient)
  - Correction:
    - **1st step: same as transient**
    - **2nd step: similar to permanent (mostly task-migration)**

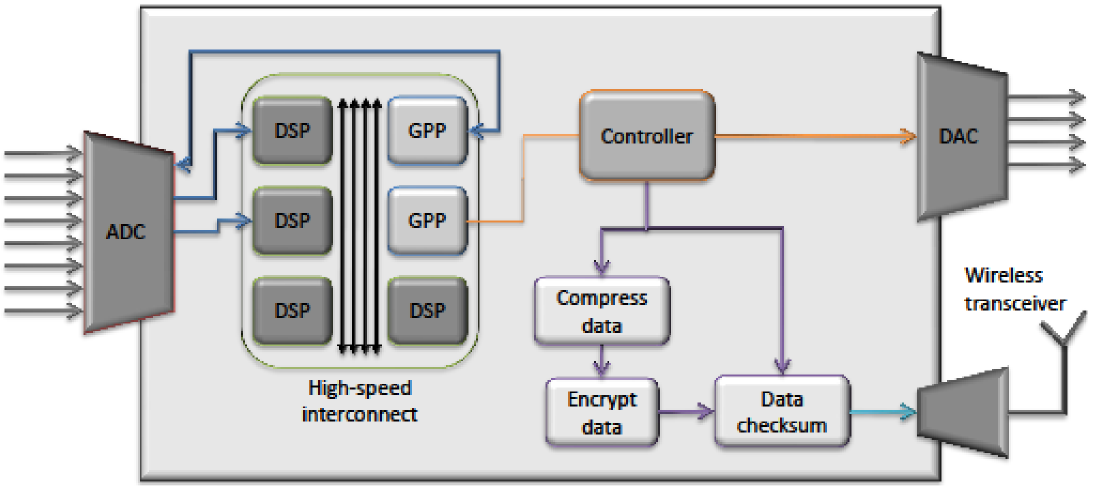
Applications

- **Two Medical SoCs**
  - Applications provided by Neurasmus BV
    - **Implantable Artificial Pancreas**
    - **Wearable Artificial Cerebellum**
  - Very high reliability constraints
  - Different power efficiency requirements
  - Different processing requirements

Artificial Cerebellum

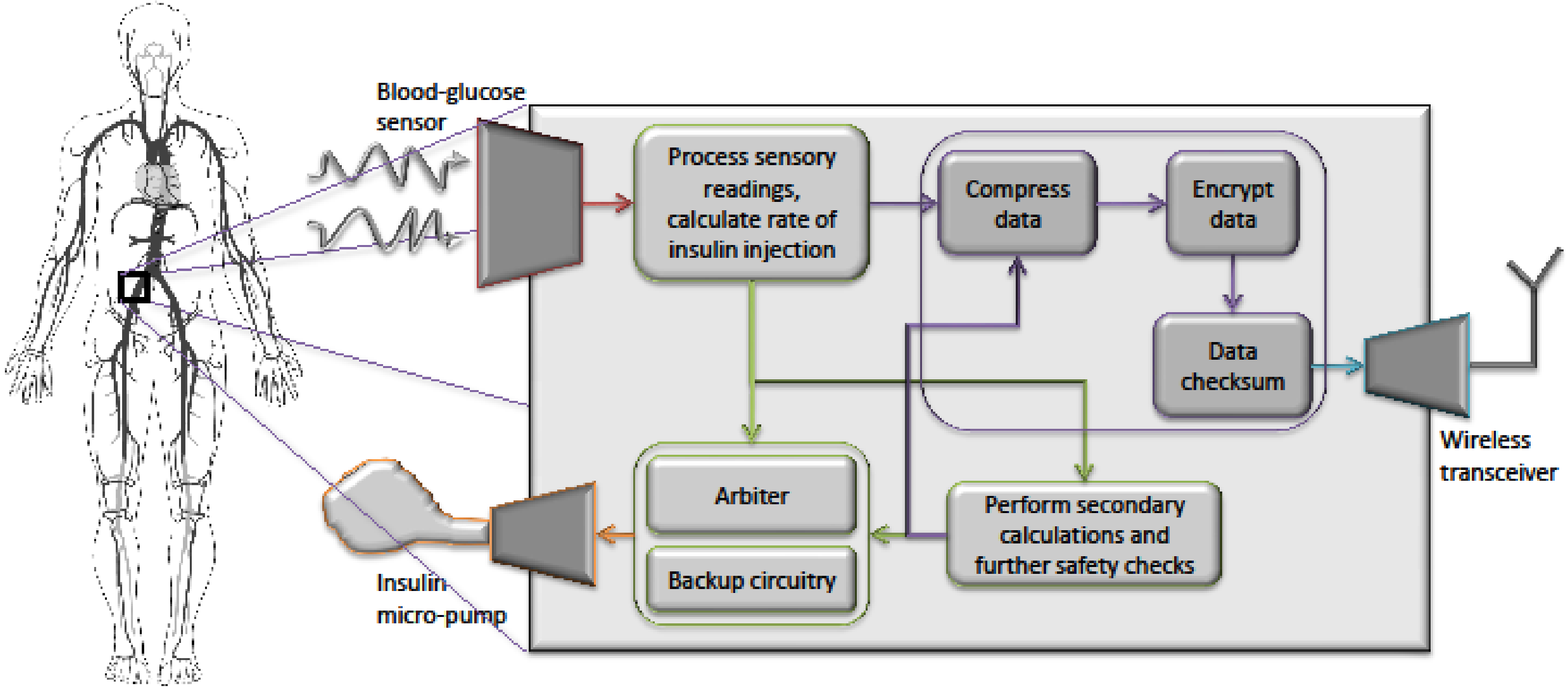

Cerebellar inputs
Purkinje cells (PC)
Recording multi-electrode site (A)
+
-
Climbing fiber
Deep cerebellar nuclear (DCN) neurons
+
Disrupted nucleo-olivary projection
To thalamic and brainstem targets
-
Stimulating multi-electrode array (B)
Inferior-olive (IO) neurons

- Replace damaged parts of the brain cerebellum
  - ❑ **recovering sensorimotor control**
- Build an artificial cerebellar system
  - ❑ **Multi-level, closed-loop control**
  - ❑ Use **Deep-Cerebellar-Nuclear-Neuron models** to artificially compute the output of the replaced part.



- Realtime constraints:
  - ❑ **Low latency**
  - ❑ **High throughput**
- High reliability
- Power efficiency
- Adaptive to different input patterns

Artificial Pancreas



- Glucose-level sensing
- Control insulin injection
- Lightweight processing
- Ultra-low power
- Wireless (and secure) user interface

Conclusions

- DeSyRe will describe a design framework for reliable future SoCs
  - **Lowering the cost of Fault tolerance**
    - **Power**
    - **Energy,**
    - **Performance**

- On-demand adaptation to
  - Fault types and densities
  - System constraints
  - Application requirements

- DeSyRe SoCs will exploit
  - The flexibility of a reconfigurable substrate
  - Runtime System support for adaptation

Thank you!

Questions?

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www.DeSyRe.eu